

Edgecore ASGvOLT-64

Open GPON-OLT Specification

Revision 1.0



OPEN
Compute Project

Revision History

Revision	Date	Author	Description
1.0	7/29/2019	Jeff Catlin	Initial Release

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	ASGvOLT-64
CPU sub-system	CPU: Intel Pentium D1519 1.5GHz DDR SDRAM: 8GB x 2 2133MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB (primary/2nd) SPI Flash (LAN): 4MB USB to NAND Flash memory : 8GB SLC (Reserve) mSATA: 32GB MLC (Reserve) m.2: 32GB MLC (TS32ZBTMM1600 TRANSCEND) CPLD: Altera 5M1270ZF256 TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45/SFP)
MAC	Broadcom BCM88470, 300Gbs full duplex switching
PON MAC	Broadcom BCM68622
BMC	AST2400
Ethernet Ports	2x QSFP28 + 8x SFP28
PON Ports	64x G-PON ports
CPLD	Altera 5M2210ZF324C5N (FBGA324 package)
FPGA	Altera 10M08DCU324C8G Altera EP4CGX15F169
PCB	20-Layers, TUC TU-883 for Mainboard 12-Layers, TG 180 for CPU module 8- Layers, TU-662 、EM-825 for BMC Board 4-Layers, FR4, Tg 150 (TU662) FAN Board
Power Supply	650W PSU front to back airflow, AC to DC, 1+1 redundant load-sharing, hot-swappable
Cooling	4 fan-tray modules with 4 pcs of 61.95mm x60.5mm x 121.9mm 12V fans, hot-swappable
Dimension	600 mm (L: Depth) x 477mm (W: Width) x 89 mm (H: Height maximum)

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Scope

This document outlines the technical specifications for the Edgecore ASGvOLT-64 Open GPON-OLT submitted to the Open Compute Foundation.

Overview

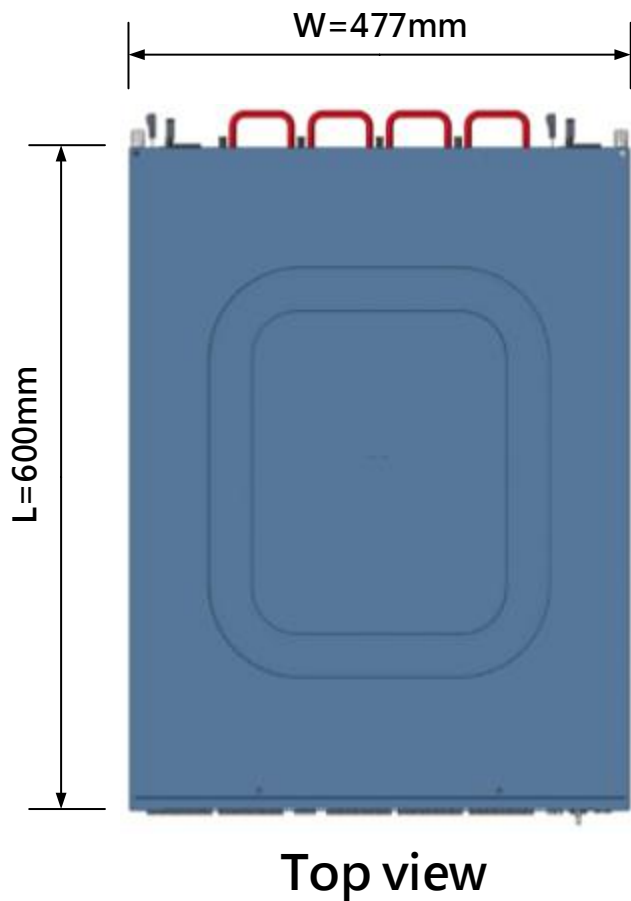
The ASGvOLT-64 supports 64*G-PON ports with 2*100G/40G QSFP28 and 8* 25G/10G SFP28 fixed ports. All G-PON ports, 100G and 25 ports, combo Management ports (SFP/RJ-45) and console/USB ports are placed on the front panel.

All G-PON ports are wire-speed and support standard G-PON SFP transceivers. The QSFP28 ports support 100G/40G operation and each QSFP28 port can be configured as 1x100GbE, 1x40GbE or 4x25GbE, 4x10GbE by using break out cables. The SFP28 ports support 25G/10G operation.

This ASGvOLT-64 supports redundant hot-swappable power supplies and redundant hot-swappable fans with front to back airflow direction.

1. Hardware Architecture

1.1. Overview





Front view

	ASFG964BBX-0818-EC
CPU sub-system	CPU: Intel Pentium D1519 1.5GHz DDR SDRAM: 8GB x 2 2133MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB (primary/2nd) SPI Flash (LAN): 4MB USB to NAND Flash memory : 8GB SLC (Reserve) mSATA: 32GB MLC (Reserve) m.2: 32GB MLC (TS32ZBTMM1600 TRANSCEND) CPLD: Altera 5M1270ZF256 TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45/SFP)
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PON MAC	Broadcom BCM68622
BMC	AST2400
Ethernet Ports	2x QSFP28 + 8x SFP28
PON Ports	64x G-PON ports
CPLD	Altera 5M2210ZF324C5N (FBGA324 package)
FPGA	Altera 10M08DCU324C8G Altera EP4CGX15F169
PCB	20-Layers, TUC TU-883 for Mainboard 12-Layers, TG 180 for CPU module 8- Layers, TU-662、 EM-825 for BMC Board 4-Layers, FR4, Tg 150 (TU662) FAN Board
Power Supply	650W PSU front to back airflow, AC to DC, 1+1 redundant load-sharing, hot-swappable
Cooling	4 fan-tray modules with 4 pcs of 61.95mm x60.5mm x 121.9mm 12V fans, hot-swappable
Dimension	600 mm (L: Depth) x 477mm (W: Width) x 89 mm (H: Height maximum)

Table 1 System Overview

1.2. Block Diagram

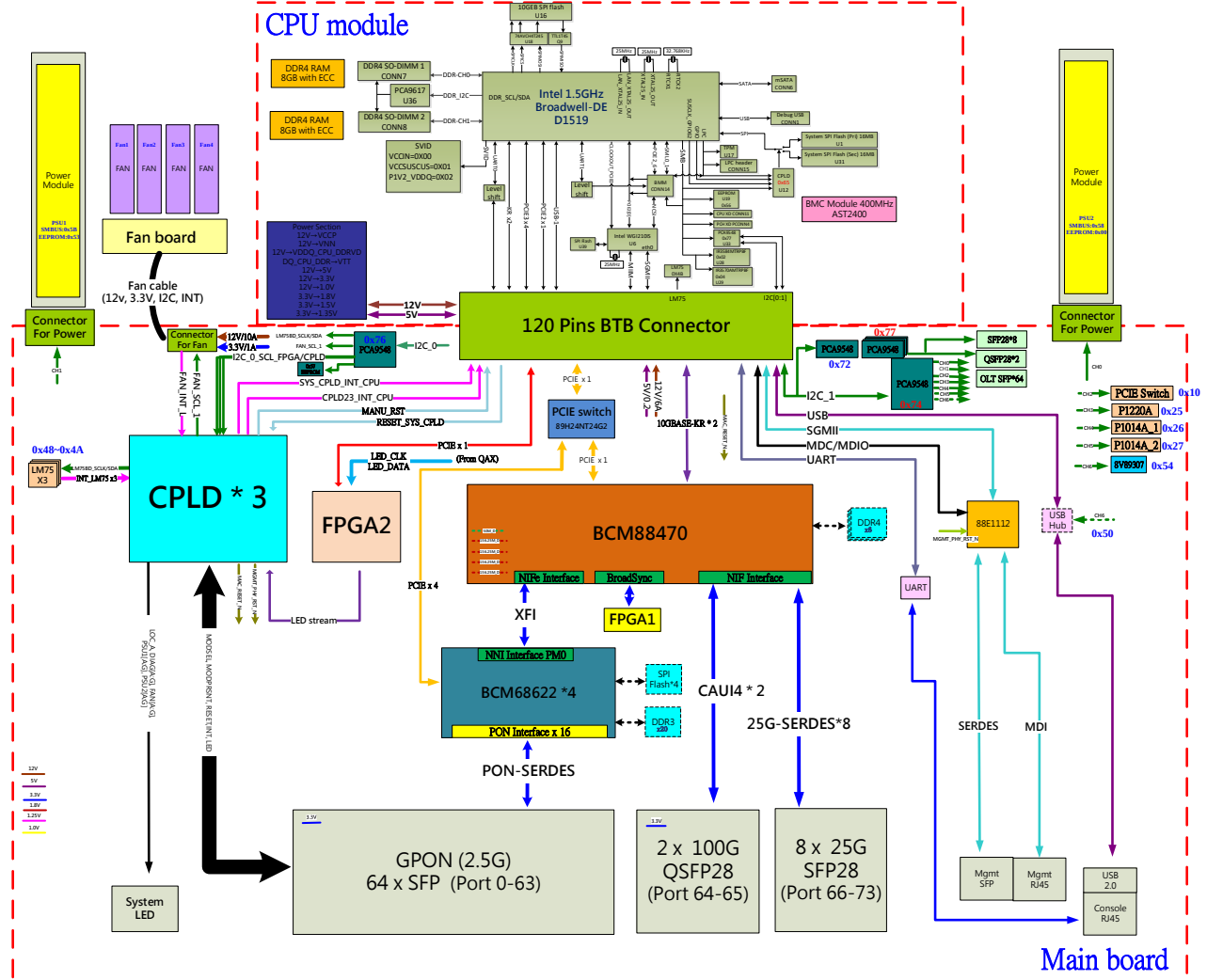


Figure 1 Block Diagram of OLT

The high-level CPU module block diagram is shown as below

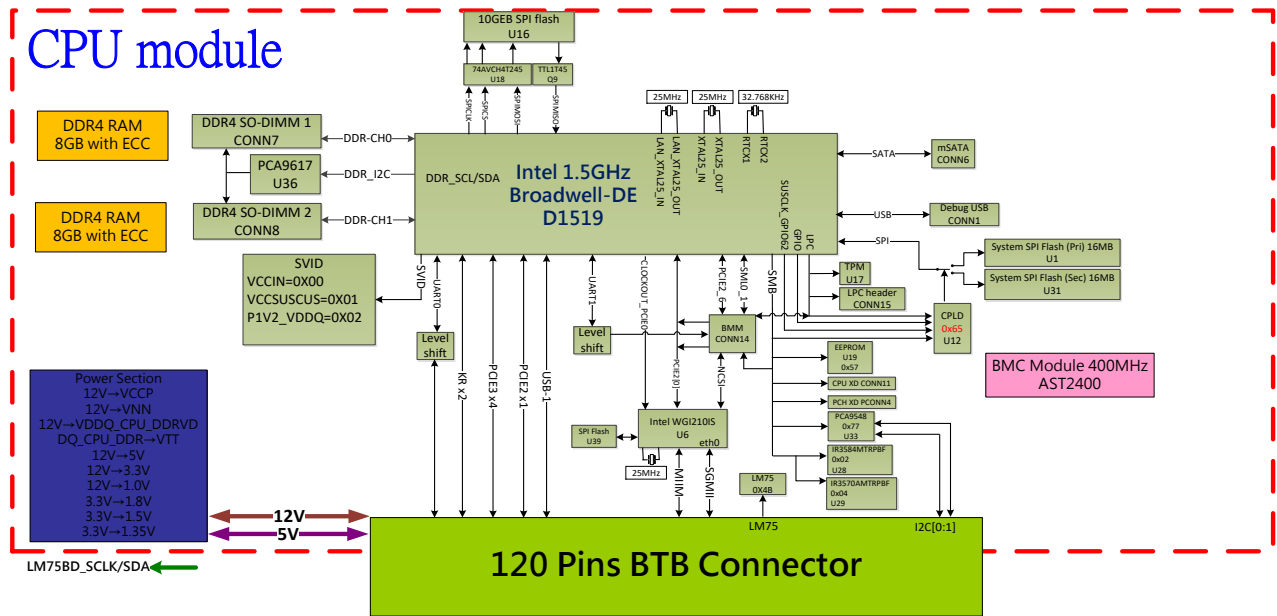


Figure 2 Block Diagram of CPU board

1.2.1. Clock Tree

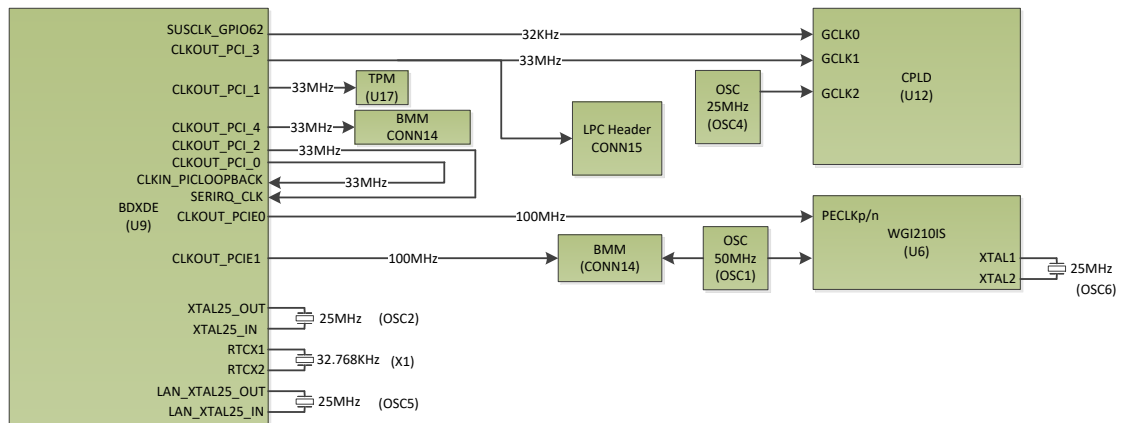
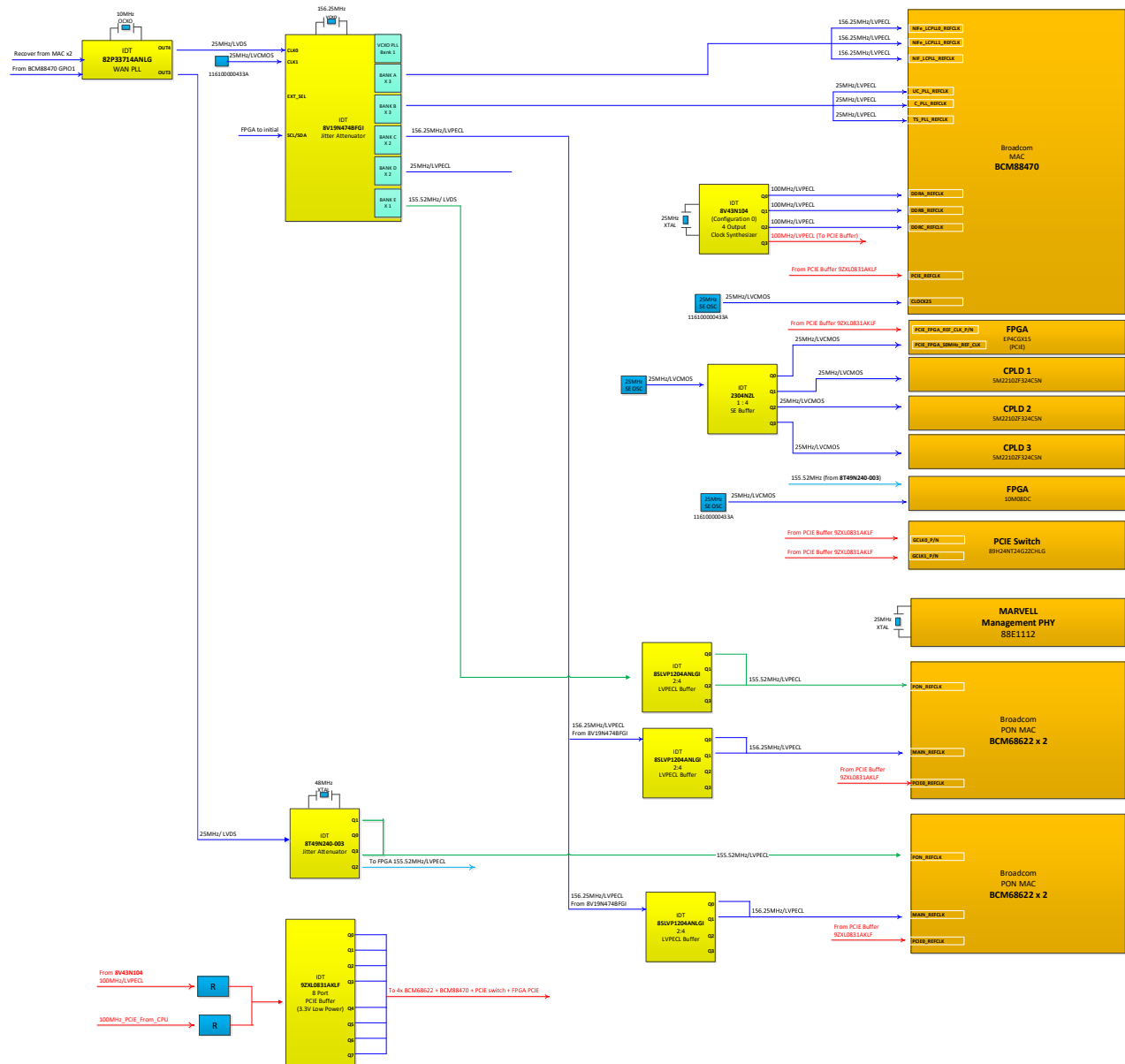


Figure 3 CPU Clock Tree



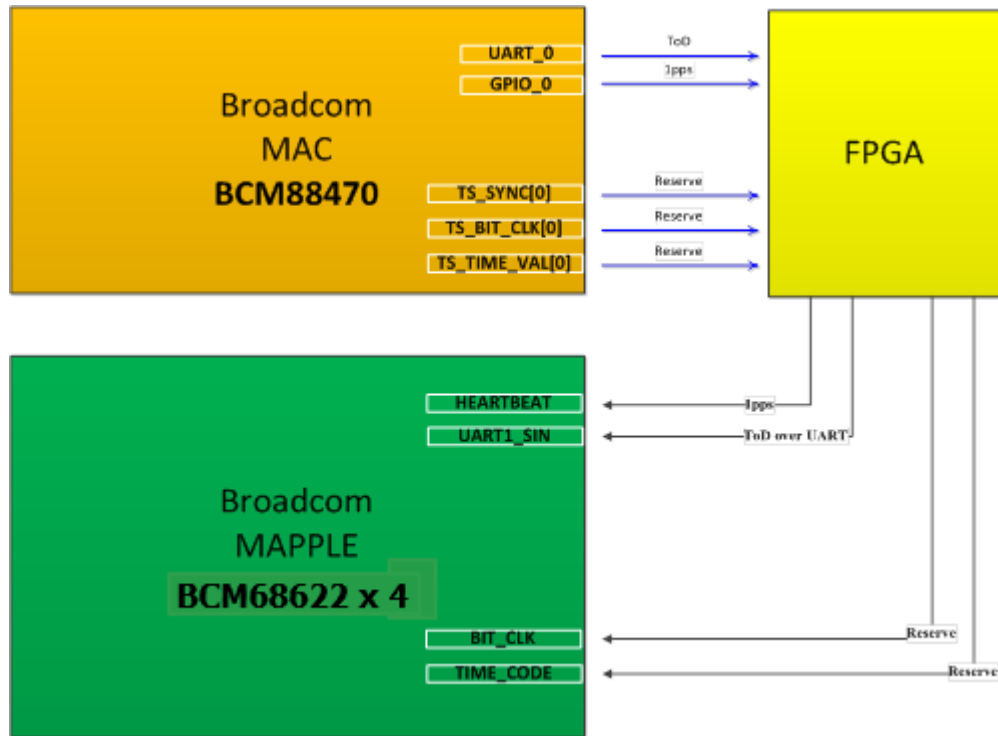


Figure 4 Mainboard Clock Tree

1.2.2. Power Tree

The power monitor and sequence controlled by the CPLD and there are three regulators that SVID interface need to support VR12.5 of Intel.

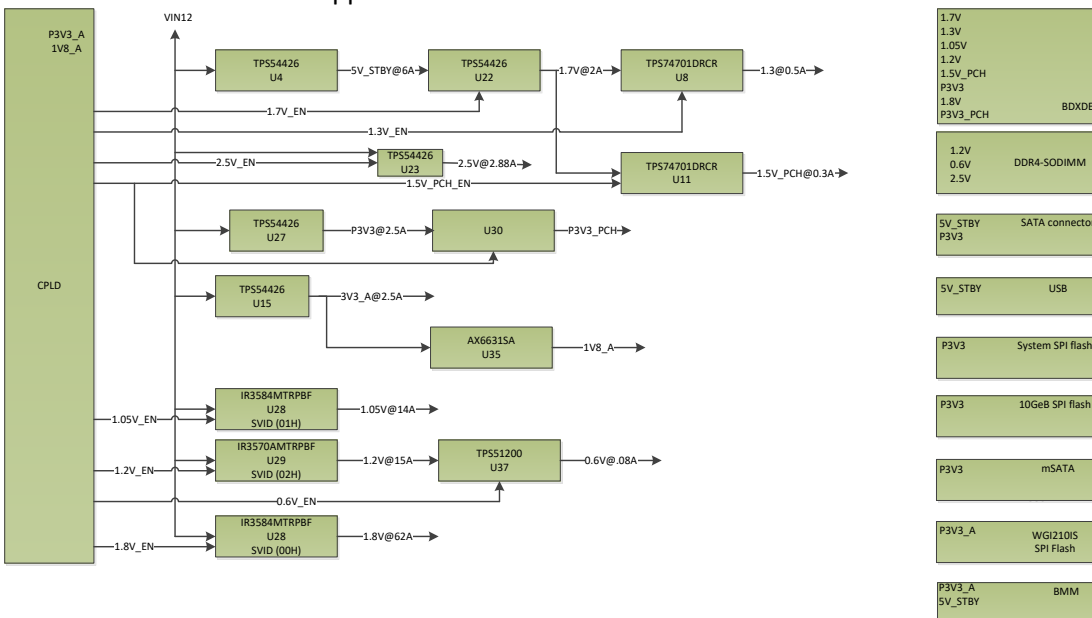


Figure 5 CPU Power Tree

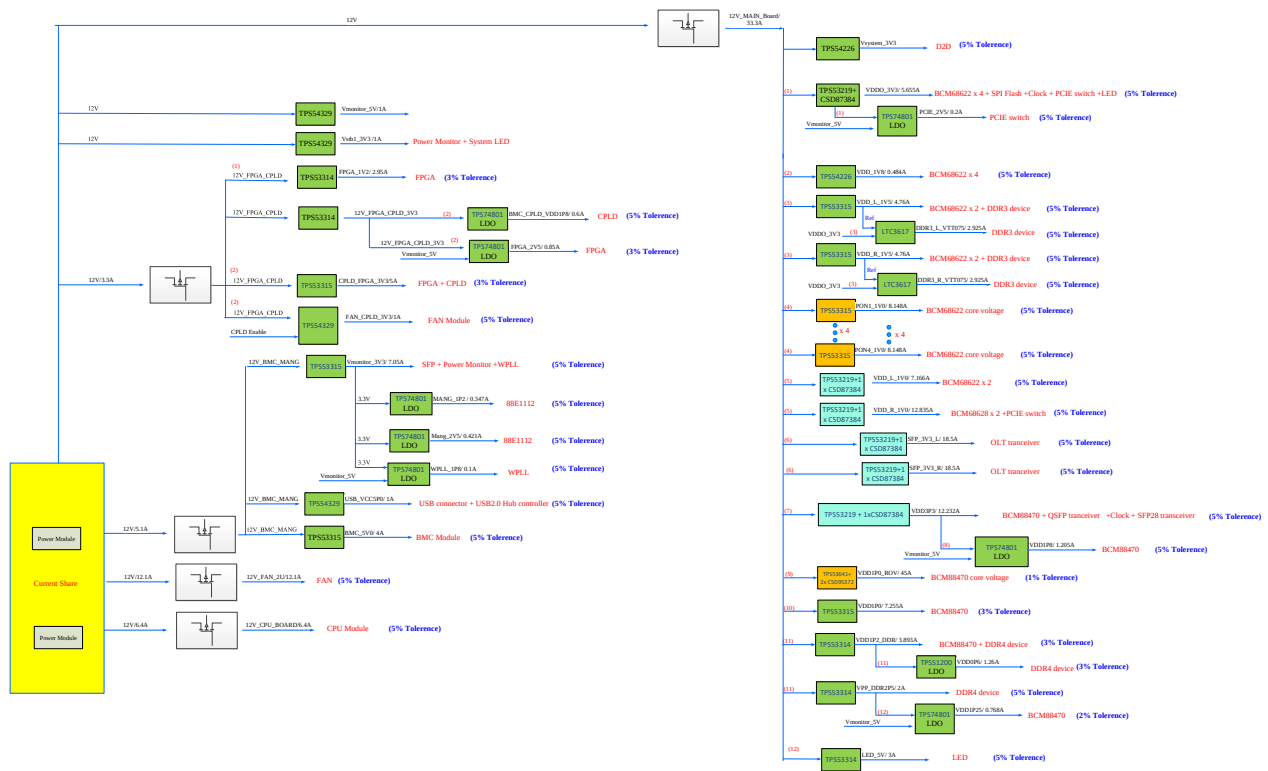


Figure 6 Mainboard Power Tree

1.2.3. Reset Tree

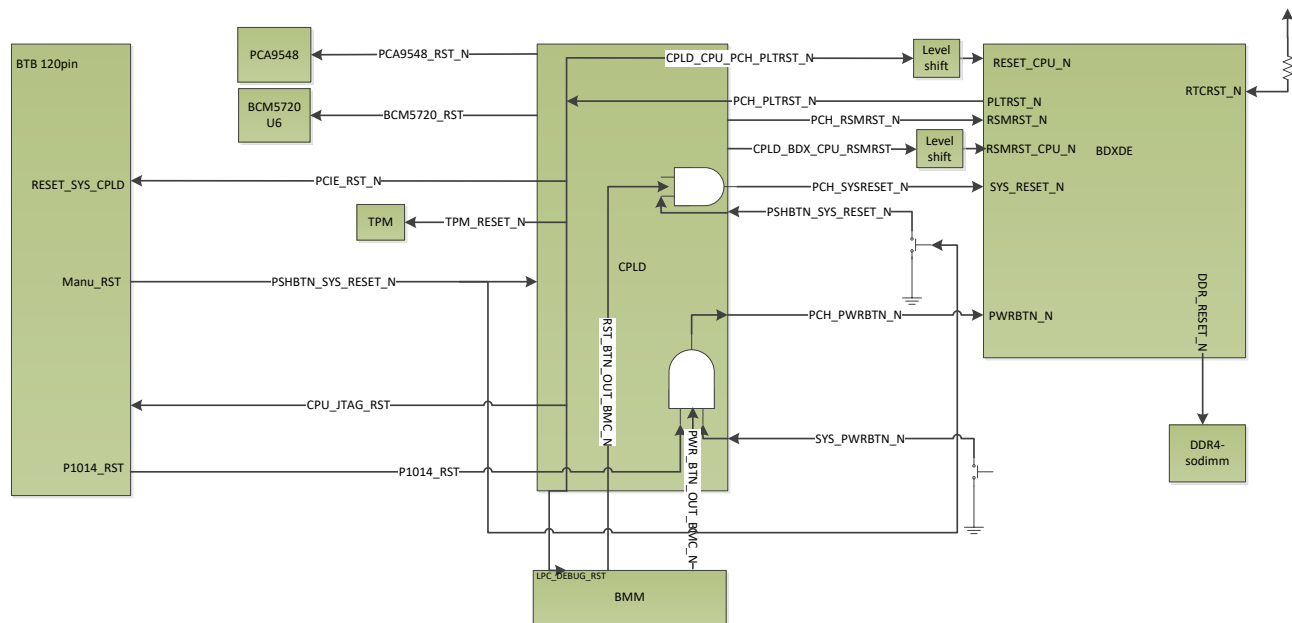


Figure 7 CPU Reset Tree

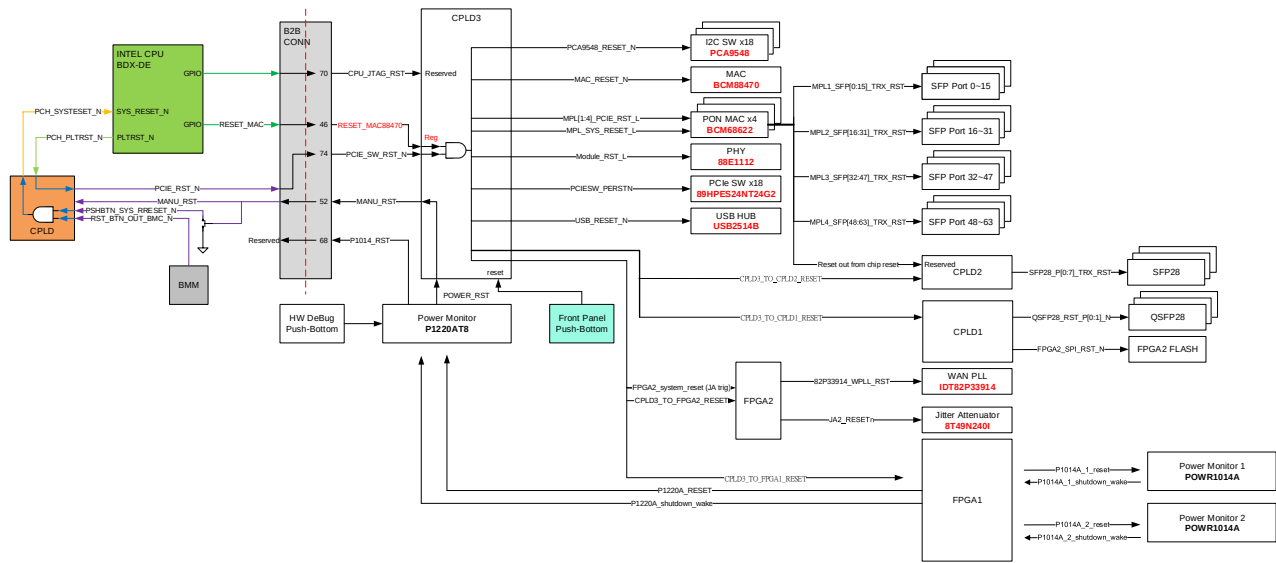


Figure 8 Main Board Reset Tree

1.2.4. Interrupt Tree

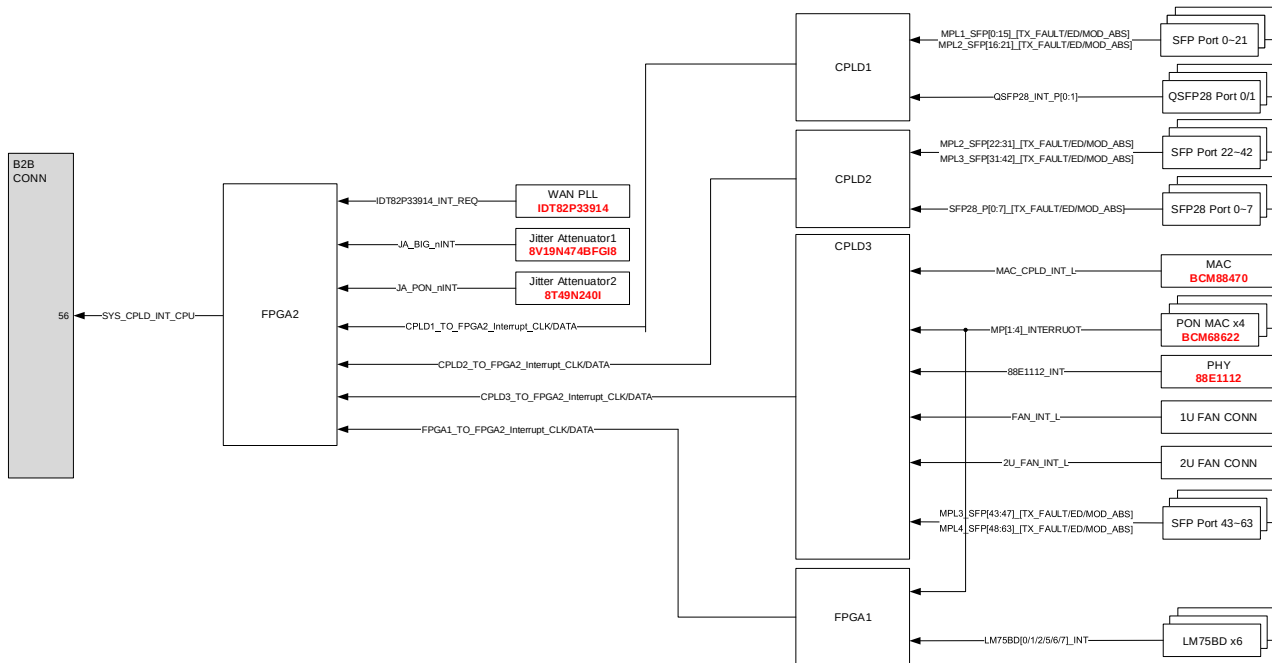


Figure 9 Main Board Interrupt Tree

1.2.5. Power up/down Sequence

There are three chips that need concern about power up/down sequence in this system. One is MAC (BCM88470), BCM68622, and the other one is CPU (BDX-DE).

The BCM88470 requires an explicit power ramp and reset sequence. 3.3V supply rails should come up first, then 1.8V and Core VDD come up later. SerDes rails should come up last while 1.25V SerDes rail should not ramp earlier than any other SerDes rails as shown in **Figure 10**. Since the

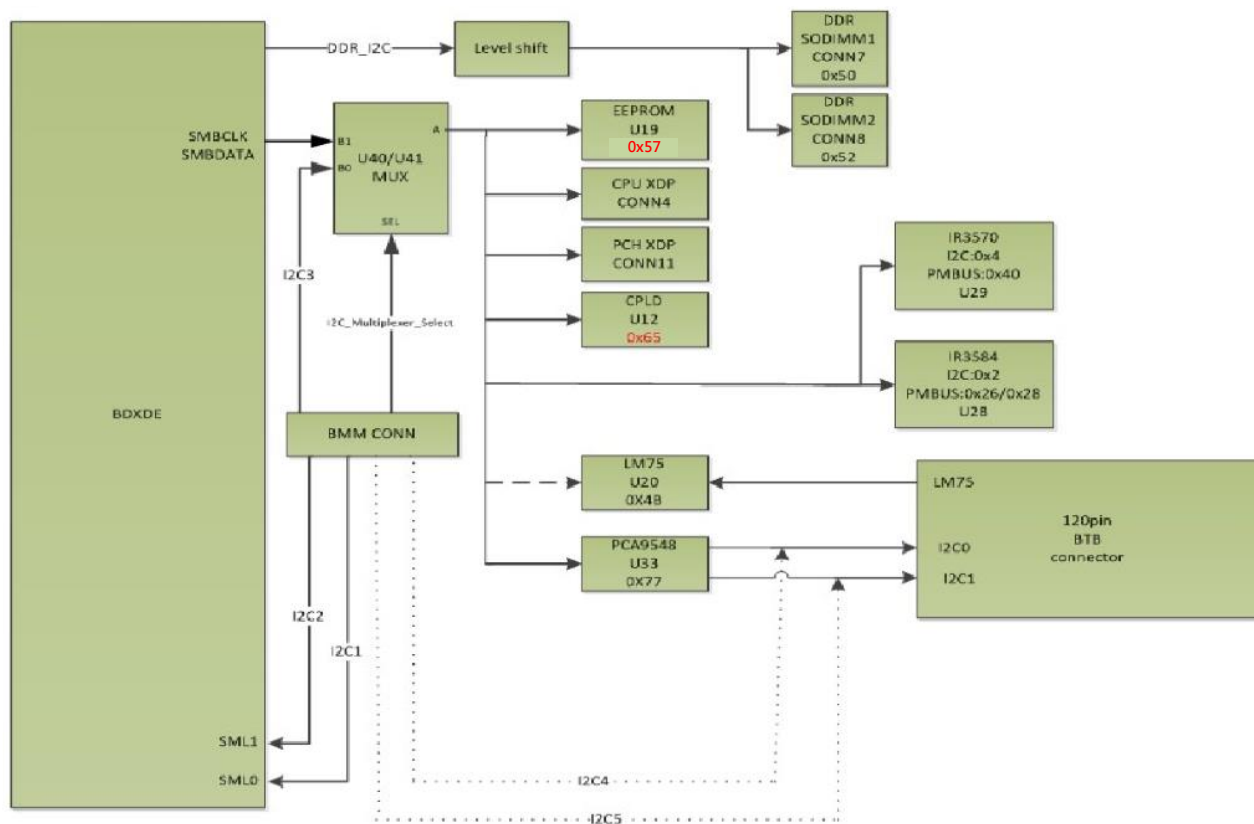


Figure 12 CPU I2C Architecture

Device	I2C address	Note
DDR4 SODIMM 1	0x50	Accessed by DDR_I2C interface
DDR4 SODIMM 2	0x52	Accessed by DDR_I2C interface
LM75	0x4B	Accessed by main board CPLD Not display at SMBus 0.
EEPROM	0x57	
IR3584 (I2C)	0x02	
IR3584 (PMBUS-Loop1)	0x26	
IR3584 (PMBus-Loop2)	0x28	
IR3570 (I2C)	0x4	
IR3570 (PMBus Loop1)	0x40	

1.4. NIF/NIFE Port Mapping

Below are the port mapping between MAC BCM88470 and front port number

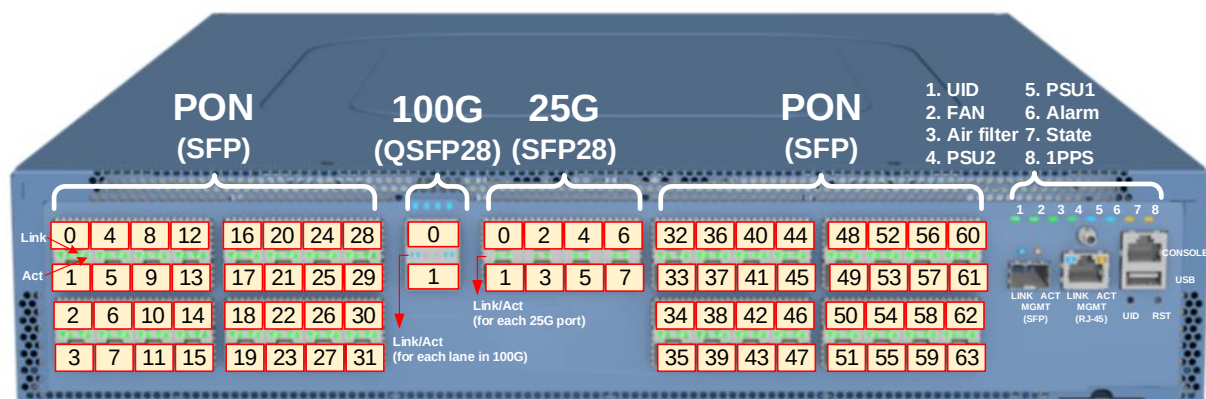


Figure 14 Front Port Mapping

MAC (BCM88470)			Front Port No.	BCM68622			
PM#	Interface	Front Port Type		Device	NNI	PON	PON NI
PM25-0	NIF_TX/RX[00]_P/N	QSFP28	100G 0	LANE 3			
	NIF_TX/RX[01]_P/N			LANE 1			
	NIF_TX/RX[02]_P/N			LANE 2			
	NIF_TX/RX[03]_P/N			LANE 0			
PM25-1	NIF_TX/RX[04]_P/N	QSFP28	100G 1	LANE 2			
	NIF_TX/RX[05]_P/N			LANE 0			
	NIF_TX/RX[06]_P/N			LANE 3			
	NIF_TX/RX[07]_P/N			LANE 1			
PM25-2	NIF_TX/RX[15]_P/N	SFP28	25G 0				
	NIF_TX/RX[14]_P/N	SFP28	25G 1				
	NIF_TX/RX[13]_P/N	SFP28	25G 2				
	NIF_TX/RX[12]_P/N	SFP28	25G 3				
PM25-3	NIF_TX/RX[11]_P/N	SFP28	25G 4				
	NIF_TX/RX[10]_P/N	SFP28	25G				

			5				
	NIF_TX/RX[09]_P/N	SFP28	25G 6				
	NIF_TX/RX[08]_P/N	SFP28	25G 7				
PM10Q-6	NIFE_TX/RX[24]_P/N	PON	6	MAPLE 1	PM0_TD/RD[0]_P/N	PON0_RD/TD[0]_P/N	7
		PON	7	MAPLE 1		PON0_RD/TD[1]_P/N	6
		PON	2	MAPLE 1		PON1_RD/TD[0]_P/N	3
		PON	3	MAPLE 1		PON1_RD/TD[1]_P/N	2
	NIFE_TX/RX[25]_P/N	PON	4	MAPLE 1	PM1_TD/RD[0]_P/N	PON0_RD/TD[2]_P/N	5
		PON	5	MAPLE 1		PON0_RD/TD[3]_P/N	4
		PON	0	MAPLE 1		PON1_RD/TD[2]_P/N	1
		PON	1	MAPLE 1		PON1_RD/TD[3]_P/N	0
PM10Q-5	NIFE_TX/RX[22]_P/N	PON	13	MAPLE 1	PM2_TD/RD[0]_P/N	PON2_RD/TD[0]_P/N	12
		PON	12	MAPLE 1		PON2_RD/TD[1]_P/N	13
		PON	9	MAPLE 1		PON3_RD/TD[0]_P/N	8
		PON	8	MAPLE 1		PON3_RD/TD[1]_P/N	9
	NIFE_TX/RX[23]_P/N	PON	15	MAPLE 1	PM3_TD/RD[0]_P/N	PON2_RD/TD[2]_P/N	14
		PON	14	MAPLE 1		PON2_RD/TD[3]_P/N	15
		PON	11	MAPLE 1		PON3_RD/TD[2]_P/N	10
		PON	10	MAPLE 1		PON3_RD/TD[3]_P/N	11
	NIFE_TX/RX[20]_P/N	PON	22	MAPLE 2	PM0_TD/RD[0]_P/N	PON0_RD/TD[0]_P/N	7
		PON	23	MAPLE 2		PON0_RD/TD[1]_P/N	6
		PON	18	MAPLE 2		PON1_RD/TD[0]_P/N	3
		PON	19	MAPLE 2		PON1_RD/TD[1]_P/N	2
	NIFE_TX/RX[21]_P/N	PON	20	MAPLE 2	PM1_TD/RD[0]_P/N	PON0_RD/TD[2]_P/N	5
		PON	21	MAPLE 2		PON0_RD/TD[3]_P/N	4
		PON	16	MAPLE 2		PON1_RD/TD[2]_P/N	1
		PON	17	MAPLE 2		PON1_RD/TD[3]_P/N	0
PM10Q-4	NIFE_TX/RX[19]_P/N	PON	29	MAPLE 2	PM2_TD/RD[0]_P/N	PON2_RD/TD[0]_P/N	12
		PON	28	MAPLE 2		PON2_RD/TD[1]_P/N	13
		PON	25	MAPLE 2		PON3_RD/TD[0]_P/N	8
		PON	24	MAPLE 2		PON3_RD/TD[1]_P/N	9
	NIFE_TX/RX[18]_P/N	PON	31	MAPLE 2	PM3_TD/RD[0]_P/N	PON2_RD/TD[2]_P/N	14
		PON	30	MAPLE 2		PON2_RD/TD[3]_P/N	15
		PON	27	MAPLE 2		PON3_RD/TD[2]_P/N	10

		PON	26	MAPLE 2		PON3_RD/TD[3]_P/N	11
PM10Q-9	NIFE_TX/RX[36]_P/N	PON	38	MAPLE 3	PM0_TD/RD[0]_P/N	PON0_RD/TD[0]_P/N	7
		PON	39	MAPLE 3		PON0_RD/TD[1]_P/N	6
		PON	34	MAPLE 3		PON1_RD/TD[0]_P/N	3
		PON	35	MAPLE 3		PON1_RD/TD[1]_P/N	2
	NIFE_TX/RX[38]_P/N	PON	36	MAPLE 3	PM1_TD/RD[0]_P/N	PON0_RD/TD[2]_P/N	5
		PON	37	MAPLE 3		PON0_RD/TD[3]_P/N	4
		PON	32	MAPLE 3		PON1_RD/TD[2]_P/N	1
		PON	33	MAPLE 3		PON1_RD/TD[3]_P/N	0
	NIFE_TX/RX[37]_P/N	PON	45	MAPLE 3	PM2_TD/RD[0]_P/N	PON2_RD/TD[0]_P/N	12
		PON	44	MAPLE 3		PON2_RD/TD[1]_P/N	13
		PON	41	MAPLE 3		PON3_RD/TD[0]_P/N	8
		PON	40	MAPLE 3		PON3_RD/TD[1]_P/N	9
	NIFE_TX/RX[39]_P/N	PON	47	MAPLE 3	PM3_TD/RD[0]_P/N	PON2_RD/TD[2]_P/N	14
		PON	46	MAPLE 3		PON2_RD/TD[3]_P/N	15
		PON	43	MAPLE 3		PON3_RD/TD[2]_P/N	10
		PON	42	MAPLE 3		PON3_RD/TD[3]_P/N	11
PM10Q-10	NIFE_TX/RX[43]_P/N	PON	54	MAPLE 4	PM0_TD/RD[0]_P/N	PON0_RD/TD[0]_P/N	7
		PON	55	MAPLE 4		PON0_RD/TD[1]_P/N	6
		PON	50	MAPLE 4		PON1_RD/TD[0]_P/N	3
		PON	51	MAPLE 4		PON1_RD/TD[1]_P/N	2
	NIFE_TX/RX[42]_P/N	PON	52	MAPLE 4	PM1_TD/RD[0]_P/N	PON0_RD/TD[2]_P/N	5
		PON	53	MAPLE 4		PON0_RD/TD[3]_P/N	4
		PON	48	MAPLE 4		PON1_RD/TD[2]_P/N	1
		PON	49	MAPLE 4		PON1_RD/TD[3]_P/N	0
	NIFE_TX/RX[41]_P/N	PON	61	MAPLE 4	PM2_TD/RD[0]_P/N	PON2_RD/TD[0]_P/N	12
		PON	60	MAPLE 4		PON2_RD/TD[1]_P/N	13
		PON	57	MAPLE 4		PON3_RD/TD[0]_P/N	8
		PON	56	MAPLE 4		PON3_RD/TD[1]_P/N	9
	NIFE_TX/RX[40]_P/N	PON	63	MAPLE 4	PM3_TD/RD[0]_P/N	PON2_RD/TD[2]_P/N	14
		PON	62	MAPLE 4		PON2_RD/TD[3]_P/N	15
		PON	59	MAPLE 4		PON3_RD/TD[2]_P/N	10
		PON	58	MAPLE 4		PON3_RD/TD[3]_P/N	11

For 16 x GPON lanes, use:

- Software PON NI ID (GPON) 2, 3, 6, 7. (BCM98620S PON front panel # 3, 4, 7, 8.)
- Software PON NI ID (GPON) 0, 1, 4, 5. (BCM98620S PON front panel # 1, 2, 5, 6.)
- Software PON NI ID (GPON) 8, 9, 12, 13. (BCM98620S PON front panel # 9, 10, 13, 14.)
- Software PON NI ID (GPON) 10, 11, 14, 15. (BCM98620S PON front panel # 15, 16, 11, 12.)

MAC BCM88470		Device	
PM10-11	NIF_TX[44]_P/N	CPU	LAN_KR_RXP1/N1
	NIF_RX[44]_P/N	CPU	LAN_KR_TXP1/N1
	NIF_TX[47]_P/N	CPU	LAN_KR_RXP0/N0
	NIF_RX[47]_P/N	CPU	LAN_KR_TXP0/N0

Table 3 NIF/NIFE mapping Table

1.5. Led Stream Format

BCM884700 has two-wire (clock and data) LED interface is to control system LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle, this selection define the Led stream by **Error! Reference source not found..**

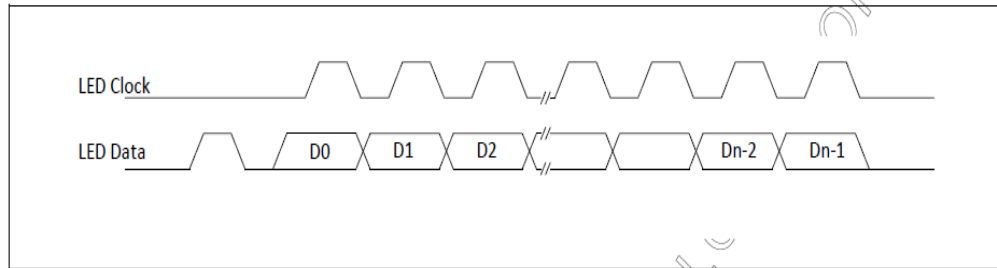


Figure 13: LED Refresh Timing

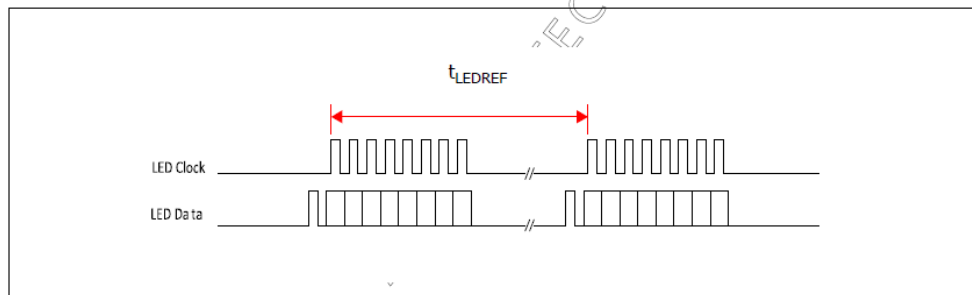


Figure 15 Led Refresh cycle

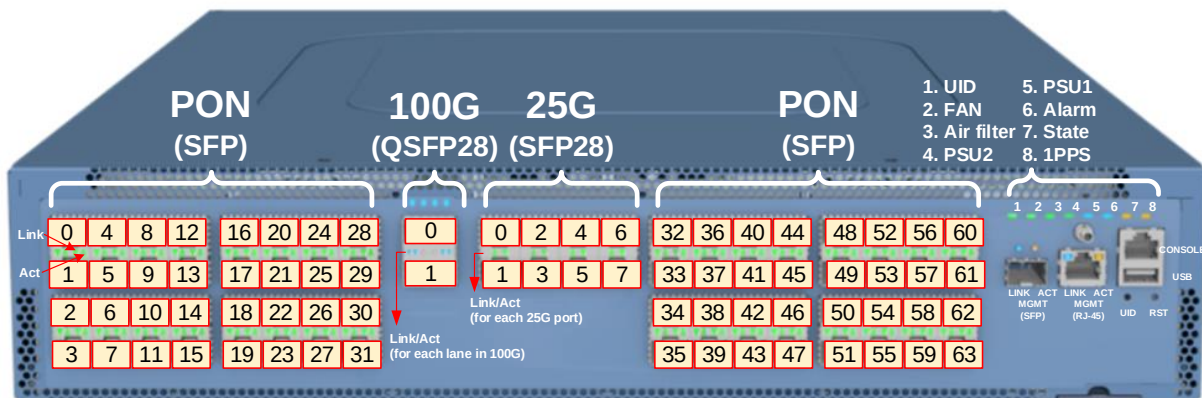


Figure 16 Front Panel Port LEDs

The status of port LED will not be affected when the switch is in configuration mode. Each port has its dedicated LED with QSFP28 and SFP28 connectors. The management port and PON port has dedicated LED to indicate Link and Activity.

LED	Description	Status
PON Link LED	LED built into SFP cage to indicate PON state	Green steady – PON link up and 1 or more ONTs Off – No ONT in service Blue – port disabled Red – fault detected
PON Activity LED	LED built into SFP cage to indicate traffic passing over the PON	Green steady - no traffic Green blinking - indicates data traffic on the PON
QSFP28 Link/Active LED	LED built into QSFP cage to indicate the pluggable status. For QSFP ports there are 4 LEDs, 1 per lane	Green – 100G or 4x25G break-out link up Blue – 40G or 4x10G break-out link up Orange – 4G or 4x1G break-out link up Off – no link <i>Noted. The LEDs blink to indicate activity.</i>
SFP28 Link/Active LED	LED built into SFP cage to indicate the pluggable status. For SFP port there are 1 LED per port.	Green – 25G link up Blue – 10G link up Orange – 1G link up Off – no link <i>Noted. The LEDs blink to indicate activity.</i>

Table 4 Port LED Definition

1.5.1. Network Ports

There are 2 x QSFP28 ports and 8x SFP28 ports on the front panel supplied by the BCM88470. These ports accept any MSA compliant QSFP28 and SFP28 pluggable supporting many link options some of which are listed below.

SFP28 connection Options

Standard	Diameter (um)	Wavelength (nm)	Distance
25GBASE-SR	Up to 100m link length with MMF link		

● QSFP28 Options

Standard	Diameter (um)	Wavelength (nm)	Distance
100GBASE-SR4	Up to 100m link length with MMF link		
100GBASE-PSM4	Up to 500m link length with SMF link		
100GBASE-LR4	Up to 10KM link length with SMF link		
100GBASE-CR4	Up to 5m with 24AWG passive DAC cable		
100GBASE-AOC	Up to 10m Active coper/optical cable		
QSFP28(100G) to QSFP (25G) fan out	● Up to 5m with passive DAC cable ● Up to 10m with Active cable		

- **10 Gigabit Ethernet SFP+ Options**

Standard	Diameter (um)	Wavelength (nm)	Distance
10GBASE-SR	Up to 300m link length with 2000 MHz*km MMF		
10GBASE-CR	Pre-terminated twin-ax copper cables with link lengths of 1m, 2m, 3m and 5m/7m		

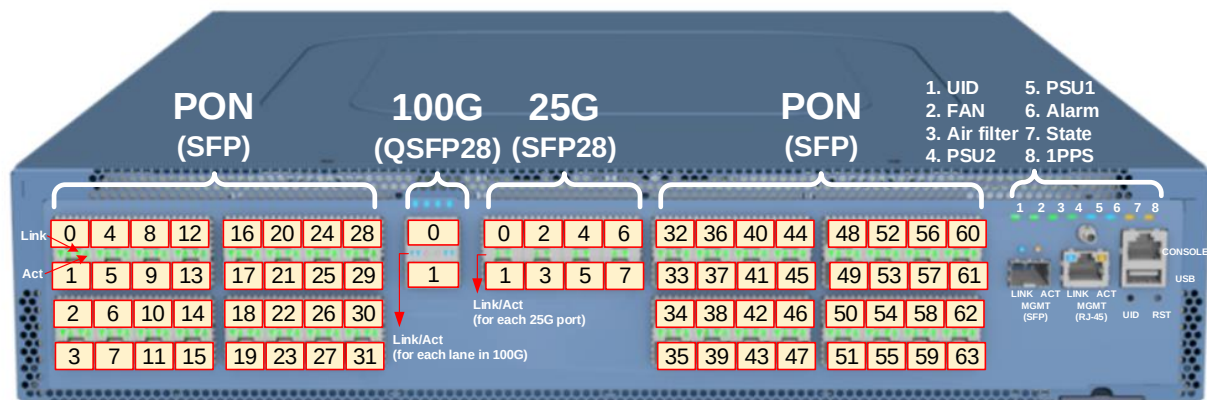
- **Does not support 10GBASE-LRM Transceiver**

- **Gigabit Ethernet SFP Options**

Standard	Diameter (um)	Wavelength (nm)	Distance
1000Base-SX	50/125	850	Finisar FTRJ8519PxNL (500M) Picolight PL-XPL-00-S13-05 (700m) Picolight PL-XPL-00-L13-21 (700m)
	62.5/125	850	Finisar FTRJ8519PxNL (300m)
1000Base-LX	50/125	1300	Agilent HFCT-5701/5710L/LP (550m)
	62.5/125	1300	Agilent HFCT-5701/5710L/LP (550m)
	9/125	1300	Finisar FTRJ-1319P1xTL (10Km)

Table 5 Types of Transceiver Supported

1.5.2. System LEDs



The system LEDs are used to indicate the status of power and system.

Label	Color	Description
State	Green	Normal
	Blue	Initializing
	Red	Fault detected
FAN	OFF	All FANS present and no FAN is FAULTY
	Red	One or more FAN is MISSING or FAULTY
PSU 1	Green	Power output available
	Red	Steady – Input power missing Blinking – Power supply failure
	Off	Power supply missing
PSU 2	Green	Power output available
	Red	Steady – Input power missing Blinking – Power supply failure
	Off	Power supply missing
Alarm	Green	Normal operation
	Blue	Minor alarm
	Red	Major alarm
UID	Blue	Blinking – “Here I am !” Off – Normal operation
1PPS	TBD	TBD
Air filter	Red	Steady – Need to change air filter Off – Air filter is clean

Table 6 System LED Definition

1.6.1. B2B Connector Pin Out

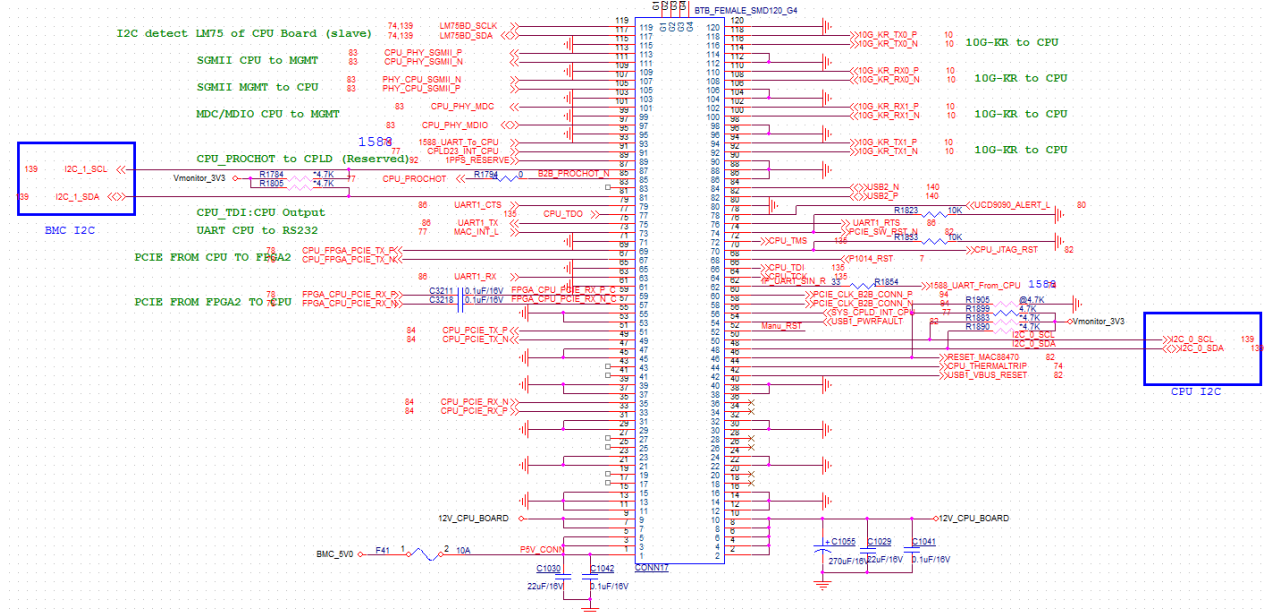


Figure 17 B2B Connector pin out

1.6.2. Fan Connector Pin Out

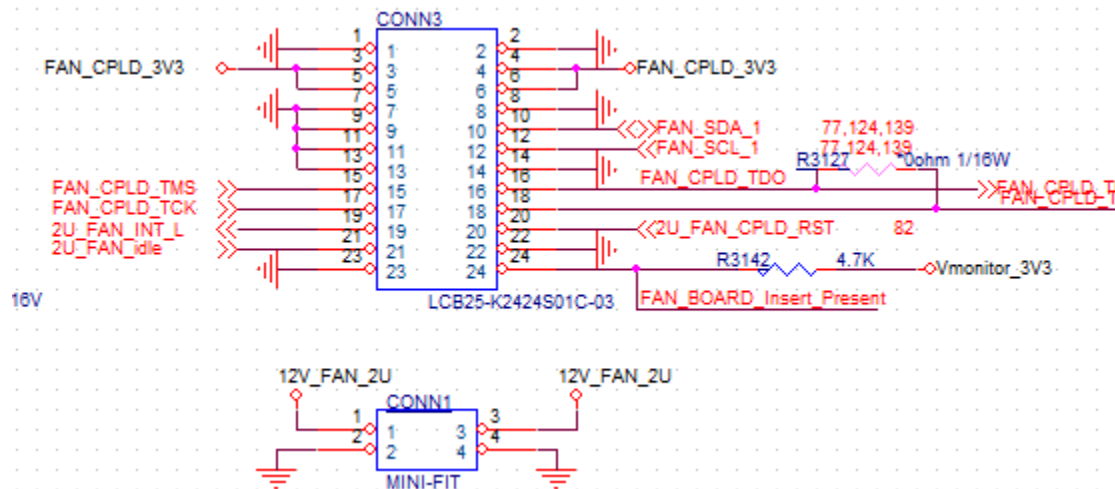


Figure 18 Fan Connector pin out

1.6.3. Console Port Pin Out

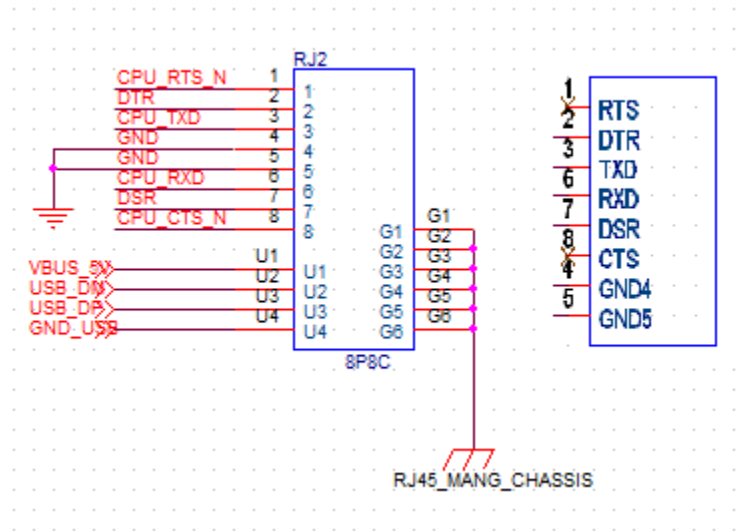


Figure 19 Console Port pin out

2. CPU/Switch Sub-system

2.1. Configurations of CPU

- 2 DDR4 channels, 1DPC with DDR4 2133 ECC SODIMM.
- Memory speed: DDR4 2133, up to 2400.
- PCI Express Lanes :
 - 24Gen3, 1x16 and 1x8, 6 controllers x4 granularity (Uncore)
 - 8 Gen2, 2x4, 8controllers x 1 granularity (Integrated PCH logic)
- Integrated 10GbE Controller contains two independent 10GbE MACs that support an XGMII interface link to the either KX4 or KR PHY device interfaces.
 - KX4 PHY supports
 - ◆ XAUI for XGMII extension
 - ◆ 10GBASE-KX4 for gigabit backplane applications.
 - ◆ 2500BASE-KX for gigabit backplane applications.
 - ◆ 1000BASE-KX for gigabit backplane applications.
 - KR PHY supports
 - ◆ 10GBASE-KR for gigabit backplane application
 - ◆ 1000BASE-KX for gigabit backplane application.
 - ◆ 10GBASE SFP+ through a XFI compatible interface
 - ◆ 10GBASE-T through a XFI compatible interface
- Integrated PCH logic
 - PCI Express Base specification, revision 2.0 support for up to eight ports with transfers up to 5GT/s
 - ACPI power management logic support revision 4.0a
 - Enhanced DMA controller, interrupt controller, and timer function.
 - Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
 - xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
 - One legacy EHCI USB controller provides a USB debug port.
 - Integrated 10/100/1000 Gigabit Ethernet MAC with system defense.

- System Management Bus (SMBus) specification, version 2.0 with additional support for I2C devices
- Supports intel Virtualization Technology for Directed I/O (Intel VT-d)
- Supports intel Trusted Execution Technology (Intel TXT)
- Integrated clock controller
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- JTAG Boundary scan support.

2.1.1. POR of CPU

The cores and uncore supports the following reset types. Note PWRGOOD_CPU is driven by the PCH.

Cold reset is the first time when the platform asserts PWRGOOD_CPU and asserts RESET_CPU_N to the uncore. The platform has to wait for the Base Clock (BCLK) and the power to be stable before asserting PWRGOOD_CPU. This results in reset of all the states in the processor, including the sticky state that is preserved on the other resets. PLLs come up, I/O (DMI2, uncore PCI Express, and DDR) links undergo initialization and calibration. Components in fixed and variable power planes are brought up. Ring, router, SAD, and various lookup tables in the core/Cbo are initialized. Once the uncore initialization has completed, then the power is enabled to the cores and cores are brought out of reset. BIOS is fetched from the PCH.

Warm reset is typically a platform wide event and is indicated by assertion and deassertion of the RESET_CPU_N signal on the socket while PWRGOOD_CPU remains asserted. This reset preserves the error log state and machine check bank states for use by platform debug. The warm reset preserves the error log state and machine check bank states for use by platform for post error event analysis. To maintain the DDR memory attached to the processor self-refresh and sticky registers remain valid through out a warm reset, the "Reset_warn" message must complete by the processor. The "Reset_warn" is a message that gets issued from the PCH to all sockets prior to warm reset. BIOS will need to program the FlexRatioMSR/CSR in each socket and invoke the Warm Reset to the platform.

The reset flow is divided into the following 5 phases.

- Phase 0: Expectations from the platform (before assertion of PWRGOOD_CPU)
 - Initially PWRGOOD_CPU signal is deasserted and RESET_CPU_N is asserted to the socket. PWRGOOD_CPU cannot deassert until RESET_CPU_N is asserted.
 - PWRGOOD_CPU must be asserted no sooner than 2 ms after the IVR Vccin supply has fully ramped-up.
 - Vccioin may be brought up before Vccin for IVR is brought up if not at the same time. Vccioin is intended to source the PECl IO.
 - The PWRGOOD_CPU and RESET_CPU_N signals have "clean" edges.
 - The reference clock (BCLK) is stable.
 - All external power rails have ramped as follows: Vccin, Vccioin, VCCD are up and stable at their nominal values
 - Assert PWRGOOD_CPU (RESET_CPU_N still asserted) only after 2 msec of Vccin, Vccioin and VCCD at tolerance.
 - After the power rails are up and stable for 2 msec and reference clocks are stable, platform asserts PWRGOOD_CPU and continues to assert RESET_CPU_N signal to the socket.

- PWRGOOD_CPU remains asserted as long as Vccin, Vccioin and VCCD remain stable.
- No power sequencing between Vccin and VCCD is required.
- Phase 1: PCU bring-up
 - Phase 1a: Activity Leading to PCU Start-up
 - ◆ Assertion of PWRGOOD_CPU (the trigger to move from the end Phase 0 to the start of Phase 1a).
 - ◆ Processor starts a timer (using BCLK) for determinism interval.
 - ◆ The PECl and SVID interfaces are held in reset until IVR asserts its power good signal.
 - ◆ The PCU PLL is enabled.
 - Phase 1b: Pcode Controlled Preparing for Broad uncore Bring-Up
 - ◆ Starting at the sub-phase, all steps should be synchronous.
 - ◆ PCU micro controller comes out of reset to start reset pcode execution. This is the planned "re-entry" point for Warm Reset processing.
 - ◆ Early reset pcode determines that it is at the start of Phase 1b.
 - ◆ Pcode brings the rest of the PCU hardware out of reset.
 - ◆ Pcode determines the boot config.
 - ◆ Pcode issues SVID command to ramp Vccin to 1.8V for cold reset.
 - ◆ Pcode reads and compares Vccin MBVR ICCMAX limit (reg 21h) vs its own supported ICCMAX limit:
 - If VR's ICCMAX $\geq$ supported ICCMAX then bootup continues.
 - If VR's ICCMAX $<$ supported ICCMAX then bootup halts and system shuts down. MSR 411h IA32_MC4_STATUS logs Error code 0x1e - MCA_VR_ICC_MAX_LESS_THAN_FUSED_ICC_MAX in field MSEC_FW.
 - ◆ Pcode sequences uncore non-boot IVRs to ramp up.
 - ◆ Pcode signals uncore power good to IIO, IMC.
 - ◆ Delivery of the uncore power good signals defines the transition from the end of phase 1b to the beginning of phase 1c.
 - Phase 1c: PLL locking and IO Calibration
 - ◆ Pcode initiates thermal sensors.
 - ◆ Pcode locks PLLs in the following order: IIO, and IMC.
 - ◆ Pcode instructs the ring PLLs to start locking.
 - ◆ RESET_CPU_N signal is deasserted.
 - ◆ De-assertion of RESET_CPU_N signal will bring PCU out of reset and signifies the transition from the end of Phase 1c to the beginning of Phase 2.
- Phase 2: Uncore initialization and core bring up
 - The starting assumptions are:
 - ◆ All IVRs except core IVRs have ramped-up and are stable.
 - ◆ All PLLs except core PLLs have locked.
 - ◆ Phase 2 is entered as a result of de-assertion of external pin RESET_CPU_N.
 - ◆ Boot mode related straps have been sampled and are available.
 - ◆ Some IO link calibration have started and may or may not have completed by the start of this phase.
 - In this phase
 - ◆ PCU comes out of reset again and again determines the reset type.
 - ◆ Reset is deasserted to the ring units (HA, Cbo, IIO).
 - ◆ Reset is de-asserted to System Agents (IMC, IIO).

- ◆ Pcode initializes the ring stops
- ◆ Pcode performs boot mode processing based on straps. Set the advertised firmware, IO, and Intel TXT agent bits appropriately.
- ◆ Pcode services DMI2 handshake protocol. If DMI2 links are used in DMI2 mode, pcode checks if the links have trained to L0. If it's the legacy socket, and if DMI2 links does not reach L0 within 3-4 ms, pcode executes error flow.
- ◆ Pcode determines number of cores, slices and st/mt-threading for the core. In this step pcode also takes into account number of BIOS-disabled cores. Pcode determines whether BIST should be executed. BIST is executed if BIST Strap is set or requested.
- ◆ Pcode programs the logical ids and switches from physical to logical mode.
- ◆ LLC reset and configuration.
- ◆ If it's not service processor boot mode, pcode waits for links to get to parameter exchange.
- ◆ Pcode releases links to get to Normal operation (i.e. L0)
- ◆ Pcode sets core Cstate to C1
- Phase 3: Reset execution (from core reset to fetch boot vector)
 - The starting assumptions are:
 - ◆ Before this phase starts, following information is provided to the core: APIC-ID, whether it's the BSP, SMT enable/disable, reset type (cold, warm, C6 exit).
 - ◆ Uncore necessary to the get to the BIOS and Intel TXT Address space is fully initialized.
 - In this phase:
 - ◆ Initialize core's internal structures, arrays, microarchitectural and architectural state.
 - ◆ Execute MLC BIST if BIST enabled.
 - ◆ Initialize uncore.
 - ◆ Read LLC BIST results from the uncore and report it in the EAX register.
 - ◆ Report LLC and MLC BIST results.
 - ◆ The core and thread selected as package BSP fetches BIOS or goes to "Wait-for-SIPI" state
 - ◆ The end assumption is there is at least one thread that was designated as package BSP.
- Phase 4: BIOS execution

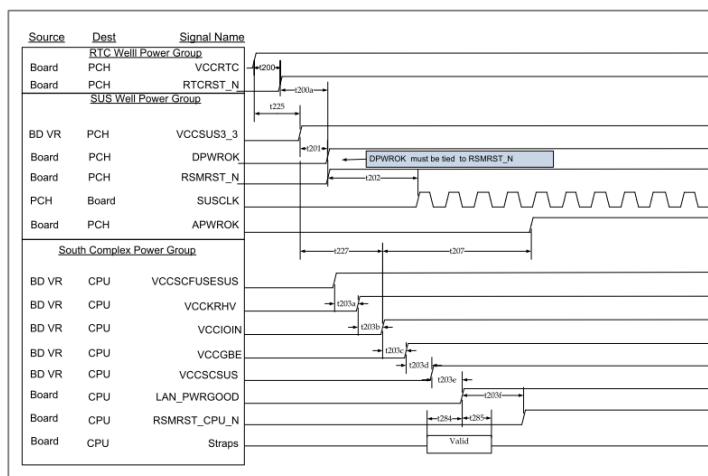


Figure 20 Power Sequencing Diagram G3 with RTC loss to S5

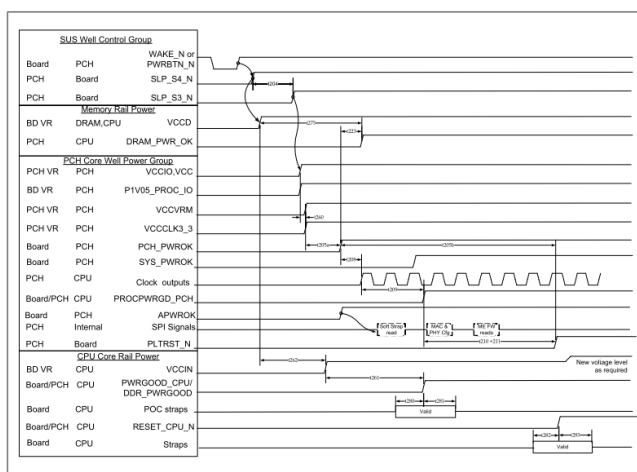


Figure 21 Power Sequencing Diagram S5 to S0

2.1.2. PCH Strap Pin Definition

Strap pin	description	value
SATA1GP/ GPIO19	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC	1
GPIO51	This field determines the destination of accesses to the BIOS memory range. Also controllable	1

	using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.	
SATA3GP /GPIO37	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	0
MFG_MODE_STRAP	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	0
INTVRMEN	0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.	1
GPIO62 / SUSCLK	0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.	1
DSWODVREN	0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.	1
SPKR	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.	
SATA2GP/GPIO36	0 = SoC RX is terminated to VSS. Grangeville platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2.	0
GPIO33	0 = SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2.	0
GPIO53	0 = SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode.	0
GPIO55	0 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. PCH will	1

	invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = Disable "Top Swap" mode.	
GPIO8	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO44	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO46	This pin must not be driven low until after rising edge of RSMRST_N.	1
BIST_ENABLE	Build-in Self-Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable	0
BMCINIT	Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled. 1 = Integrated Service Processor Boot Mode Enable	1
TXT_PLTEN	0 = The platform is not Intel TXT enabled. 1 = Default. The platform is Intel TXT enabled.	0
TXT_AGENT	0 = Default. The SoC is not the Intel TXT Agent. 1 = The SoC is the Intel TXT Agent.	0
SAFE_MODE_BOOT	0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled	1
DEBUG_EN_N	0 = Debug Mode 1 = Normal Mode	XDP_PRESENT_N
DDR3_4_STRAP	Select between DDR4 and DDR3 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)	1
PECIO ; PECI1 ; PECI2	In micro-server design space, there will be multiple sockets that share a PECE bus. However these sockets are effectively independent agents. The PECE IDs are used as straps to identify which socket is which in order for PECE bus to work.	000
LAN_MDIO_DIR_CTL_0; LAN_MDIO_DIR_CTL_1	00 = Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = Port 1 is disabled. Port 0 is enabled. 10 = Reserved 11 = Both Port 0 and 1 are enabled. Recommend 5.1K ohm pull up to VCCIOIN or 5.1K ohm pull down to GND.	11
RSVD12_AJ67	This pin should have a 5.1K ohm pull down to	0

	GND.	
RSVD11_AG67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD10_AN78	This pin should have a 5.1K ohm pull down to GND.	0
RSVD09_AC64	This pin should have a 5.1K ohm pull down to GND.	0
SERIRQ_DIR	Recommend 5.1k ohm pull up to VCCIOIN.	1
UART_TXD[0]	Recommend 5.1k ohm pull down to GND.	0
UART_TXD[1]	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_RXD0	Recommend 5.1K ohm pull up to VCCIOIN.	1
LAN_NCSI_RXD1	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = LAN not available in S5. Manageability is disabled. Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_ARB_OUT	Selects SVID VR Operating Mode 1 - VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Separate SVID controllers (default).	1
RSVD84	49.9Ω 1% to GND	0
RSVD93	1k - 5.1kΩ to GND	0
RSVD94	1k - 5.1kΩ to GND	0
RSVD00	1k - 5.1kΩ to VCC3_3	1
RSVD18	1k - 5.1kΩ to GND	0
RSVD16	1k - 5.1kΩ to GND	0
RSVD17	1k - 5.1kΩ to GND	0
RSVD21	1k - 5.1kΩ to GND	0
NCTF/TP	1k - 5.1kΩ to VCC3_3	1

Table 7 PCH Strap definitions

2.2. CPU Memory Mapping

Broadwell-DE SoC contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes Broadwell-DE SoC I/O and memory maps at the register-set level. Register access is also described.

Bus:Device:Function	Function Description
Bus0:Device31:Function0	LPC controller
Bus0:Device31:Function2	SATA controller #1
Bus0:Device31:Function3	SMBus controller
Bus0:Device31:Function5	SATA controller#2

Bus0:Device31:Function6	Thermal subsystem
Bus0:Device29:Function0	USB EHCI controller#1
Bus0:Device28:Function0	PCI-e port1
Bus0:Device28:Function1	PCI-e port2
Bus0:Device28:Function2	PCI-e port3
Bus0:Device28:Function3	PCI-e port4
Bus0:Device28:Function4	PCI-e port5
Bus0:Device28:Function5	PCI-e port6
Bus0:Device28:Function6	PCI-e port7
Bus0:Device28:Function7	PCI-e port8
Bus0:Device25:Function0	Gigabit Ethernet controller
Bus0:Device22:Function0	Intel management engine interface#1
Bus0:Device22:Function1	Intel management engine interface#2
Bus0:Device22:Function2	IDE-R
Bus0:Device22:Function3	KT
Bus0:Device20:Function0	xHCI controller

Table 8 PCI devices and functions

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC

70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Table 9 Fixed I/O ranges decoded by Broadwell-DE

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	64	Power management

IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	16	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	32	SMB unit
TCO	96 bytes above ACPI base	32	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	32	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Table 10 Variable I/O decode ranges

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC__000h-FEC__040h	IOx APIC inside broadwell-de SoC	__ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set

FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh FF80 0000h- FF87 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h- FF8F FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh FF90 0000h- FF97 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h- FF9F FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh FFA0 0000h- FFA7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFE7 FFFFh FFA8 0000h- FFAF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h-FFFF FFFFh FFB8 0000h-FFBF FFFFh	LPC or SPI (or PCI)	Always enabled. The top two 64KB blocks of this range can be swapped.
FF70 0000h-FF7F FFFFh FF30 0000h-FF3F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h-FF6F FFFFh FF20 0000h-FF2F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h-FF5F FFFFh FF10 0000h-FF1F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h-FF4F FFFFh FF00 0000h-FF0F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARA)
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARB)
1 KB anywhere in 4 GB range	USB EHCI Controller #1	Enable using standard PCI mechanism (D29:F0)
64 KB anywhere in 4 GB range	USB xHCI Controller	Enable using standard PCI mechanism (D20:F0)
FED0 X000h-FED0 X3FFh	High Precision Event Timers	BIOS determines the “fixed” location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
FED4 0000h-FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4 GB range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)

Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit [0] of the LPC Generic Memory Range register (D31:F0: offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable using standard PCI mechanism (D31:F3)
2 KB anywhere above 64 KB to 4 GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable using standard PCI mechanism (D31:F2)
Memory Base/Limit anywhere in 4 GB range	PCI Express* Root Ports 1-8	Enable using standard PCI mechanism (D28: F 0-7)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (D28:F 0-7)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBAR/ TBARH)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® MEI #1, #2	Enable using standard PCI mechanism (D22:F 1:0)
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism (D22:F3)
16 KB anywhere in 4 GB range	Root Complex Register Block (RCRB)	Enable using setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).

Table 11 Memory decode ranges from processor perspective

2.3. CPU Flash

There are four SPI flashes, 2 x 128Mb for BIOS, 1 x 32Mb for 10GBE controller +and 1 x 16Mb for WGI210IT.

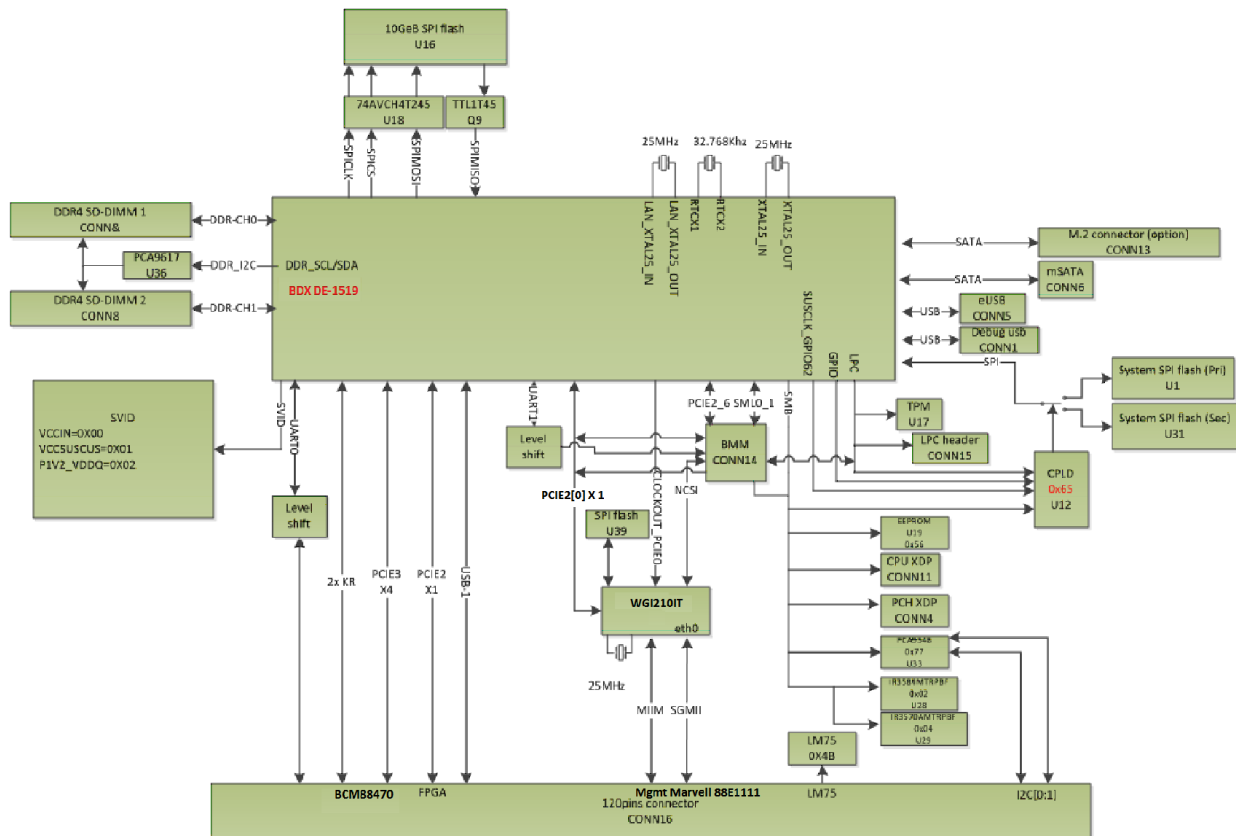
U1, U31, the two 128Mb flash are for system boot BIOS, one is primary another one is backup.

There are two ways that can update the BIOS flash, one is via dediprog (CONN3), the other is via BMC module. If user want to update bios from BMC, the “BDX_SPI_MUX_SEL” would be pull low from high.

U16, 32Mb flash is for 10G controller setup that need level shift because of that SPI interface voltage level of BDXDE LAN is 1.05volt different SPI flash voltage level.

U39, the 16Mb flash is for WGI210IT MAC setup.

The system boot flash SPI clock rate is 20MHz via the SPI memory mapped configuration register SSFC[18:16] = “000” setting and the CPU GbE LAN SPI flash clock rate is 20MHz via the GbE LAN memory mapped configuration register SSFC[18:16] = “000” setting.



2.3.1. Bios Flash Upgrade

There are two methods to upgrade the system bios flash:

- Using SF100 DEDIPROG programmer
- Using BMC module

2.3.1.1. Using SF100/SF600 DEDIPROG programmer

- ### 1. Preparing the SF100 / SF600

BIOS SPI Flash Update

- Tools Required:
 - Host Windows* PC with USB port
 - DediProg* SF600 SPI Flash Programmer
 - SF600 cable Adapter with an 8-pin header
 - USB cable
 - <http://www.dediprog.com/>
- Required Software:
 - Download and install the software corresponding to the DediProg* SF600 SPI Flash Programmer tool onto the Windows* PC
 - <http://www.dediprog.com/>



2. Select flash
 - U1: Current BIOS Image (CI)
 - U31: Known Good BIOS Image (KGI)
3. Connect the SF100/SF600 connect on CONN3
4. For CI flash, put jumper on CONN2 = 1-2
5. For KGI flash, put jumper on CONN2 = 2-3

2.3.1.2. 10GBE firmware flash upgrade

The U16 10GBE flash could be upgrade by SW

2.3.1.3. WGI210IT firmware flash upgrade

The U39 WGI210IT flash could be upgrade by SW

2.4. RAM

2.4.1. CPU RAM

The Intel Broadwell-DE CPU family can support memory DDR3 and DDR4 that need via strap pin DDR3_4_STRAP to configure which one be supported.

Currently the board supports two DDR4 SODIMM modules with ECC, so the DDR3_4_STRAP should be pull to high.

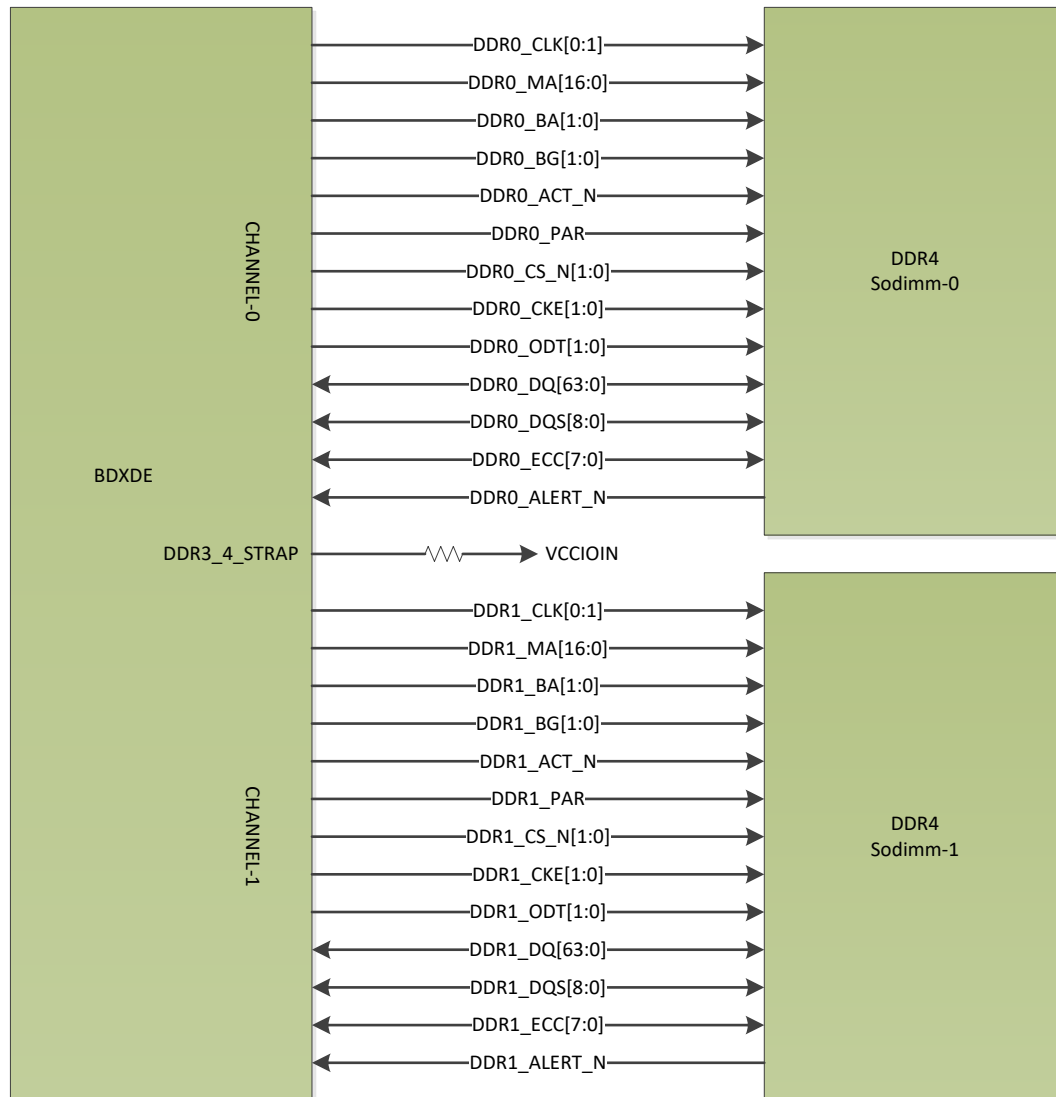
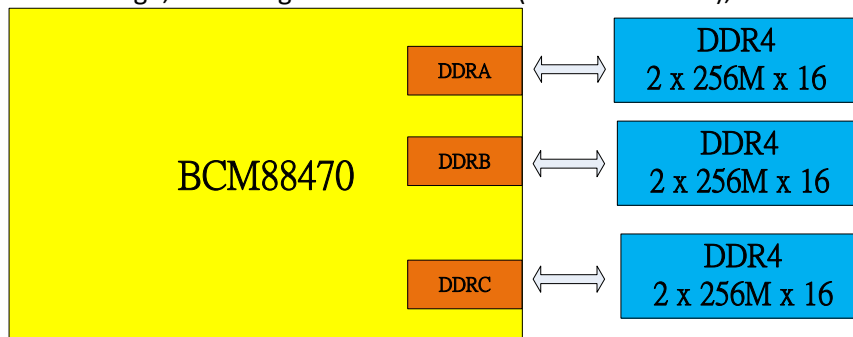


Figure 23 RAM Connection

2.4.2. BCM88470 RAM

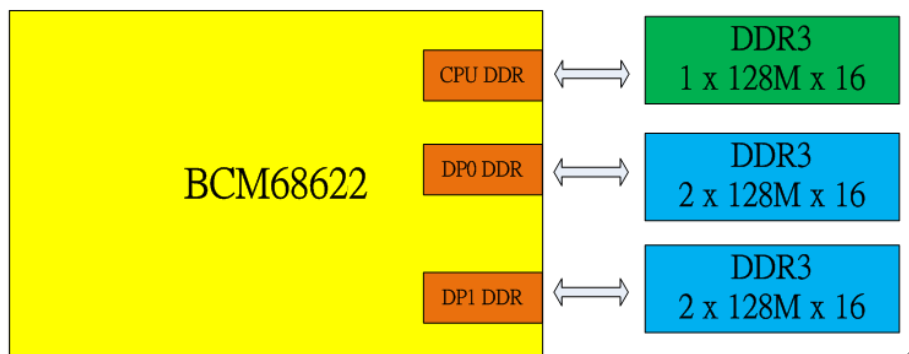
BCM88470 support three channels of DDR4/GDDR5 DRAM memory. Each channel can support up to two DDR4 devices that used separated CS signals. For DDR4 interface, 32b wide and storage capability up to 8 GB per channel. DRAM data rate of up to 3.2G for DDR4.

In our design, we configuration Full DRAM (three interfaces), see below.



2.4.3. BCM68622 RAM

Below show BCM68622 had three kind of DDR3 interface that are for CPU, DP0 and DP1. Each section can support up to DDR3-1600. For CPU DDR interface, DDR3 [0] and DDR3[1] memory configuration as below.



2.5. PCIe

The CPU board has to provide the x4 PCIe Gen3 and x1 PCIe Gen2 to B2B connector.

CPU can access Main board through x1 PCIe Gen2 that connect to PCIe switch 89H24NT24G2ZCHLG. The device side is BCM88470 and BCM68622.

PCIe GEN1 x1 is communicate the FPGA of Main board.

There are other PCIe GEN2 that connect to on board MAC I210 and BMC module.

The PCIe interface connected to I210 is PCIe GEN2 x1.

The PCIe interface connected to BMC module is PCIe GEN2 x1, which is used to active the graphic inside the BMC chip to achieve the vKVM and vMedia function through IPMI when the BMC chip uses AST2400.

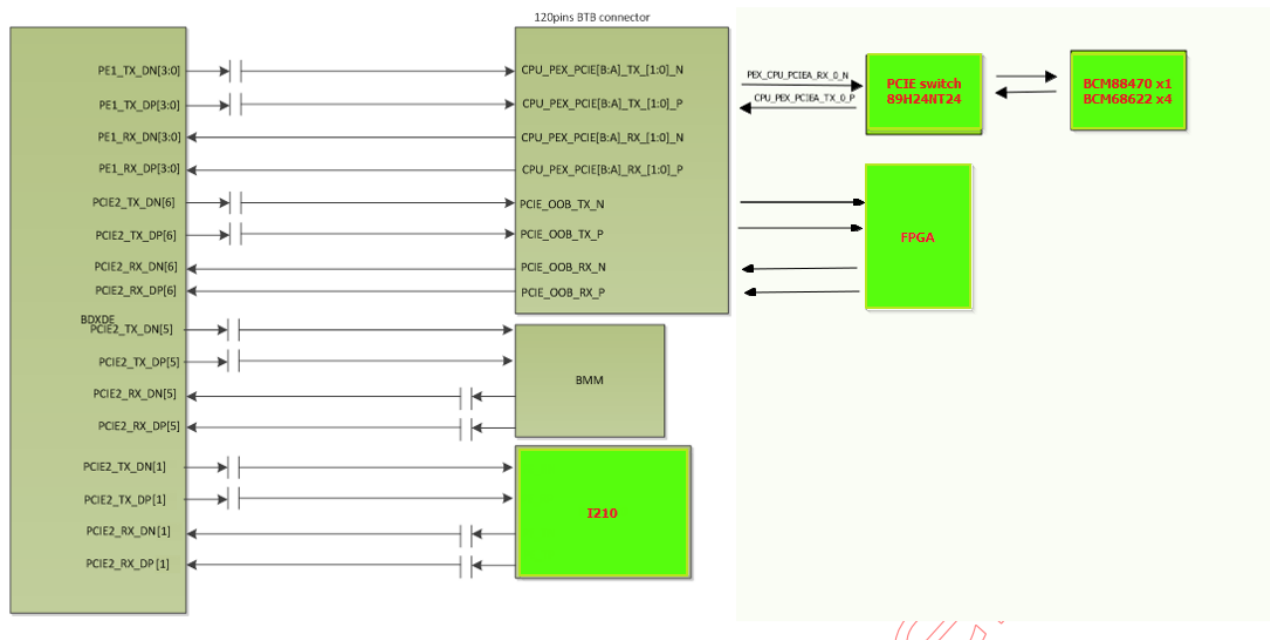


Figure 24 PCIe Topology

2.6. UART

There are two UART interfaces of Broadwell-DE CPU, UART0 and UART1.

UART0 is the main system console and connect to main board through 120pin connector and BMC via CPLD, the reason is to support the SOL function when BMC is present.

UART1 is the reserved UART interface and directly connect to BMC module.

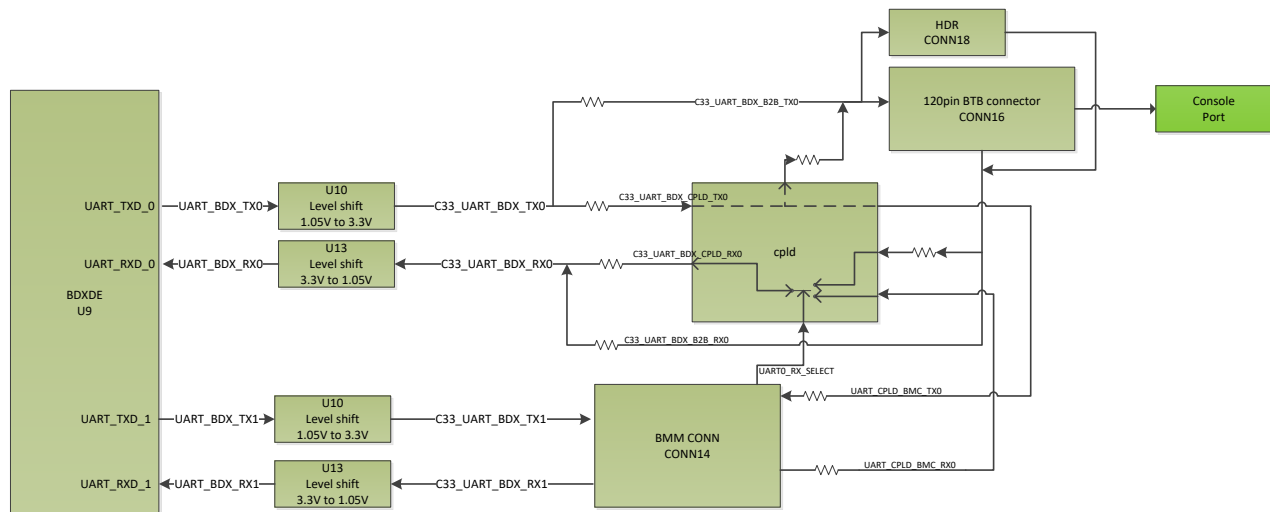


Figure 25 UART Connection

Pin Number	Description
1	VCC

2	TX
3	RX
4	GND

Table 12 CONN18 PIN ASSIGNMENT

2.7. USB

There are four USB 2.0 interfaces in the project.

The USB-0 via the 120pins BTB connector to Main board is for chassis USB connector.

The USB-1 is for debug function.

The USB-2 connects to eUSB module for OS access. (Reverse)

The USB-3 is connected to BMC module for vMEDIA function.

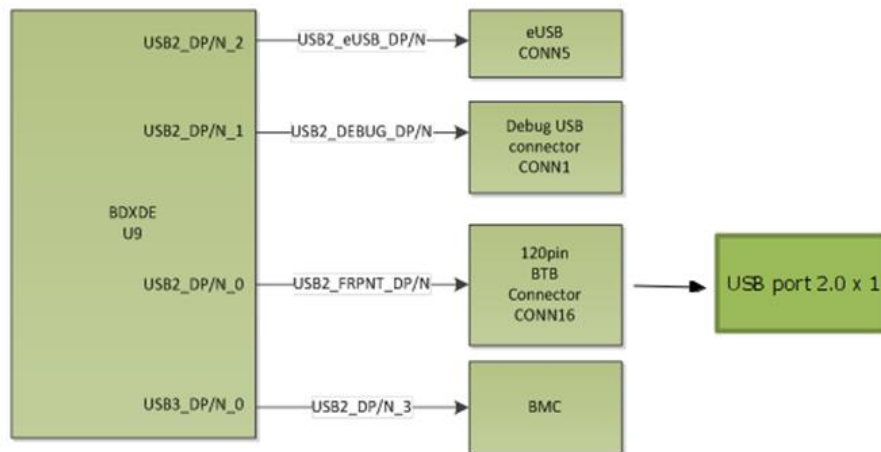


Figure 26 USB Connection

2.8. SATA

The CPU board supports 2 SATA SSD devices via SATA 3.0 interface.

SATA 3.0 CH0 support mSATA SSD module. (mSATA is reverse)

SATA 3.0 CH1 support m.2 SSD module.

The following table shows the mSATA and m.2 SSD module dimension and size.

Type	Dimension	Capacity
mSATA SSD	50.8mm x 29.85mm x 4.0mm	16GB~512GB (option)
M.2 SSD	42.0mm x 22.0mm x 3.5mm	32GB~256GB (default)
	80.0mm x 22.0mm	32GB~512GB (option)

Table 13 SATA SSD Module Table

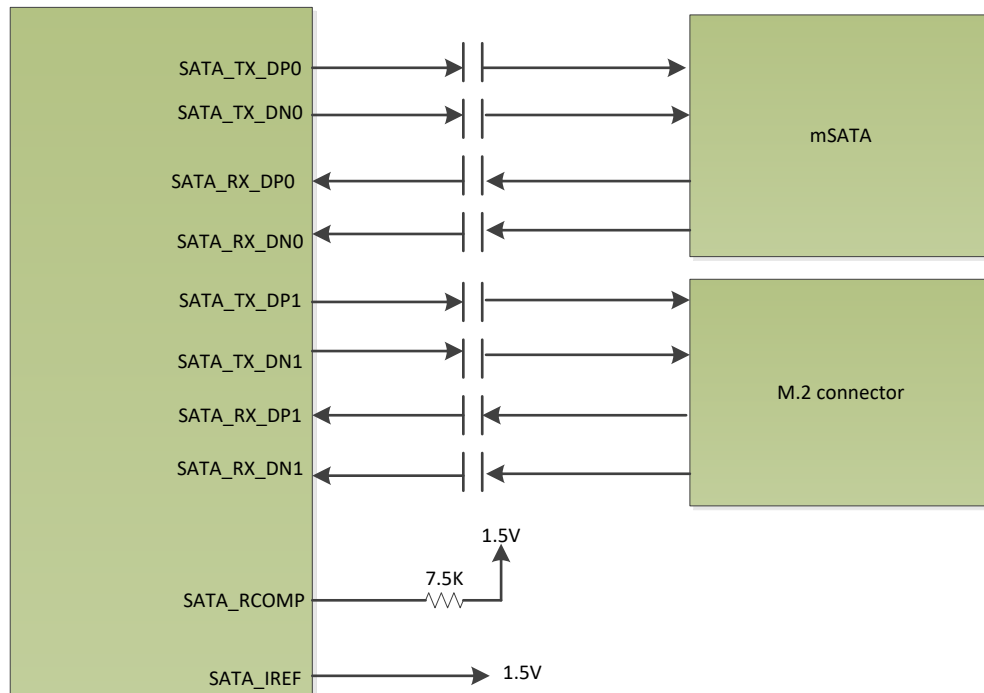


Figure 27 SATA Connection

2.9. 10G-Base-KR

The 10GBE interface of the Broadwell-DE CPU on the CPU board uses 10G-KR to communicate with the MAC BCM88470 on the main board to support additional high speed datalink between CPU and MAC.

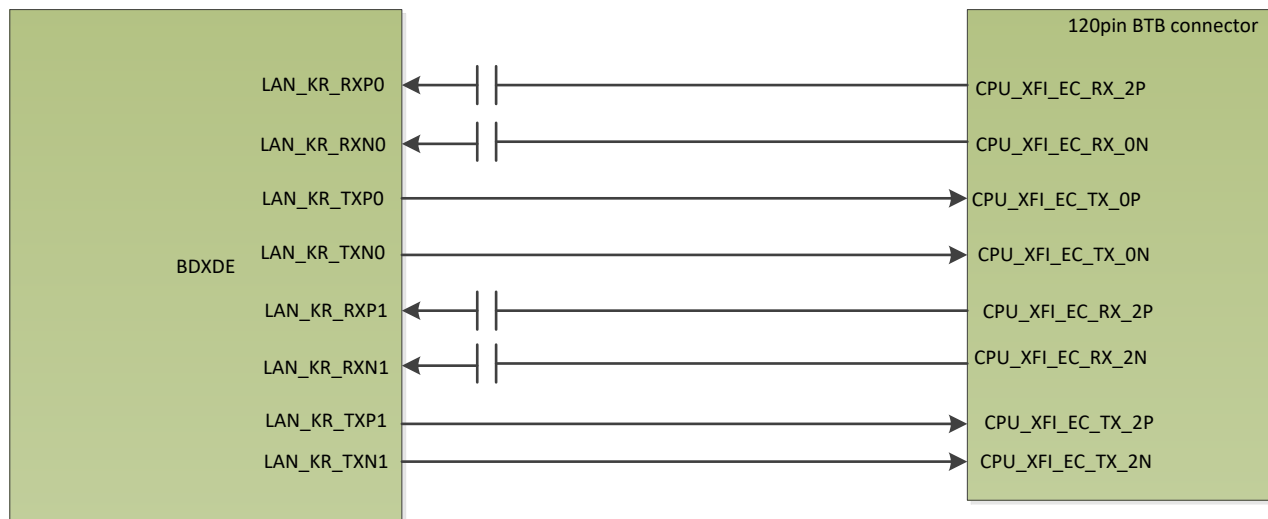


Figure 28 10GBase-KR Connection

2.10. GPIO

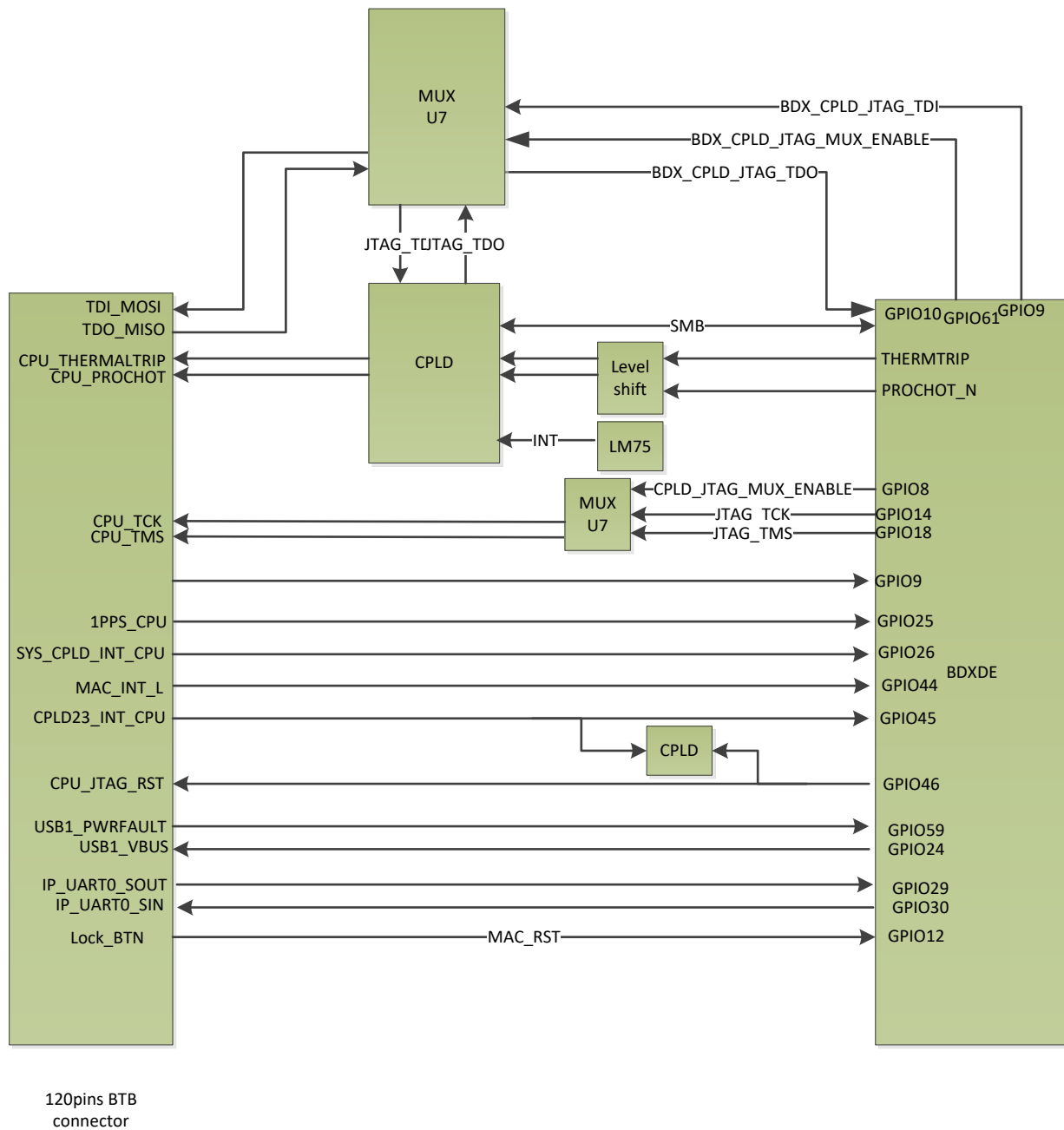


Figure 29 GPIO Connection

The following table is the GPIO function description of BDXDE CPU.

Pin name	GPIO_USE_SEL 1: GPIO 0: Native	GPIO_IO_SEL 1: input 0: output	function
GPIO0	0	X	BMBUSY#
GPIO1	1	0	Watch dog event clear indicator
GPIO2	0	X	NC
GPIO3	0	X	NC
GPIO4	1	1	CPU to PCH Throttle event interrupt
GPIO5	0	X	NC
GPIO6	1	0	JTAG enable, enable JTAG multiplexer to update CPLD code from CPU. 1: enable the JTAG multiplexer 0: disable the JTAG multiplexer
GPIO7	0	X	NC
GPIO8	1	0	JTAG Multiplexer select, which select the JTAG signals from CPU would go to CPLD or main board 1: to CPLD (default) 0: to Main board
GPIO9	1	0	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI When configure to be BDX_CPLD_JTAG_TDI, which is CPU JTAG output
GPIO10	1	1	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO When this pin configure to BDX_CPLD_JTAG_TDO , which is CPU JTAG input
GPIO11	0	X	SMBALERT#
GPIO12	1	0	Reset MAC, to do the sleep function.

GPIO14	1	0	XDP_NOA7_PCH/ BDX_CPLD_JTAG_TCK
GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/ FM_THROTTLE_N
GPIO17	1	1	BMC present detect
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	1	0	SCLOCK
GPIO23	0	X	NC
GPIO24	0	0	NC
GPIO25	1	1	1PPS_CPU
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT
GPIO29	1	0	IP_UART0_SOUT
GPIO30	1	1	IP_UART0_SIN
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	X	X	NC
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	0	SLOAD
GPIO39	0	0	SDATAOUT0
GPIO40	0	BI	XDP_NOA1_PCH
GPIO41	1	0	XDP_NOA2_PCH/

			CPLD_CONFIG_CLK
GPIO42	1	BI	XDP_NOA3_PCH/ CPLD_CONFIG_DATA
GPIO43	1	0	XDP_NOA4_PCH / ADR_MCU_INIT
GPIO44	0	1	NC
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST
GPIO48	1	0	SDATAOUT1
GPIO49	1	0	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC
GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV
GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	BI	XDP_NOA0_PCH
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	0	X	SUSCLK_33K
GPIO65	0	X	NC
GPIO67	0	X	NC
GPIO68	1	1	CPLD interrupt
GPIO69	0	X	NC
GPIO70	0	X	NC
GPIO71	0	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

Table 14 GPIO table

2.11. JTAG

The JTAG interface of the CPU board is used to upgrade the CPLD via CPU in the whole chassis, including U12 on the CPU board, other CPLDs are on the main board and FAN board.

When the CPLD on the CPU board needs to be upgraded, the GPIO8 of Broadwell-DE needs to select to “1”, and the GPIO61 needs to select to “1”.

When the CPLD devices on the main board or FAN board need to be upgrade, GPIO8 of Broadwell-DE needs to select to “0”, and the GPIO61 needs to select to “0”.

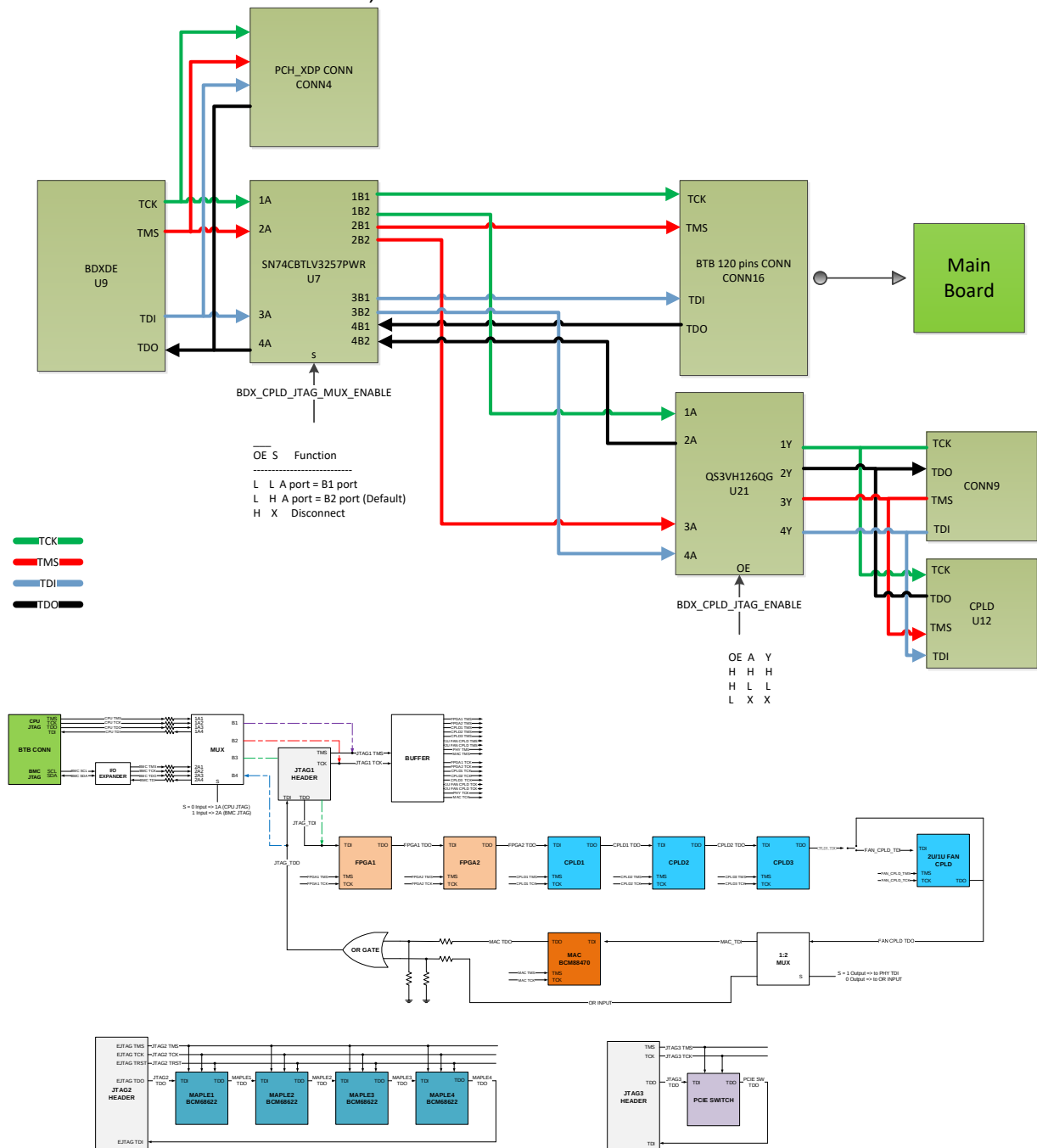


Figure 30 JTAG architecture for CPU and Main board

2.12. CPLD and FPGA

A CPLD is used for BDX-DE as the glue logic for getting some Specific system-related information and doing some system controls.

Section 3.12.1 and 3.12.2 indicates CPLD and FPGA at Main board.

Section 3.12.3 indicates CPLD at Fan Board

Section 3.12.4 indicates CPLD at CPU board.

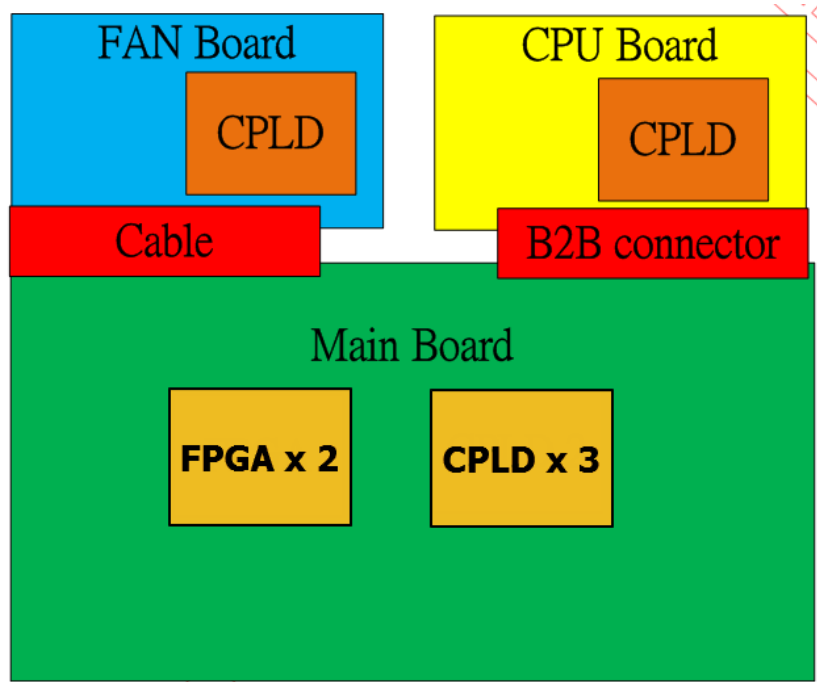


Figure 31 CPLD and FPGA

2.12.1. FPGA

FPGA is at Main Board. I2C access address see Figure 13. Please see section 2.3 for detail access method.

FPGA function as below:

1. Main Board D2D Margin High/Low control.
2. BCM88470 core voltage control (Reserve). Default is control by CPU.
3. PON LED control.
4. Access Thermal sensor by I2C.
5. Broadcast ToD message from BCM88470 to Each BCM68622. This relate to IEEE1588 (slave only).
6. Main Board Power On/Off control
7. Reset and Interrupt

FPGA upgrade by JTAG that can through external connector or CPU, please see [Figure 30](#) for detail block diagram.

Figure 32 show block diagram for Main Board Power On/Off and Margin High/Low control methods.

Figure 33 show block diagram for ToD message fan-out from BCM88470 to each BCM68622. IEEE1588 PTP message is received and processes by BCM88470 then sync each BCM68622 via ToD(over UART) and 1pps signal.

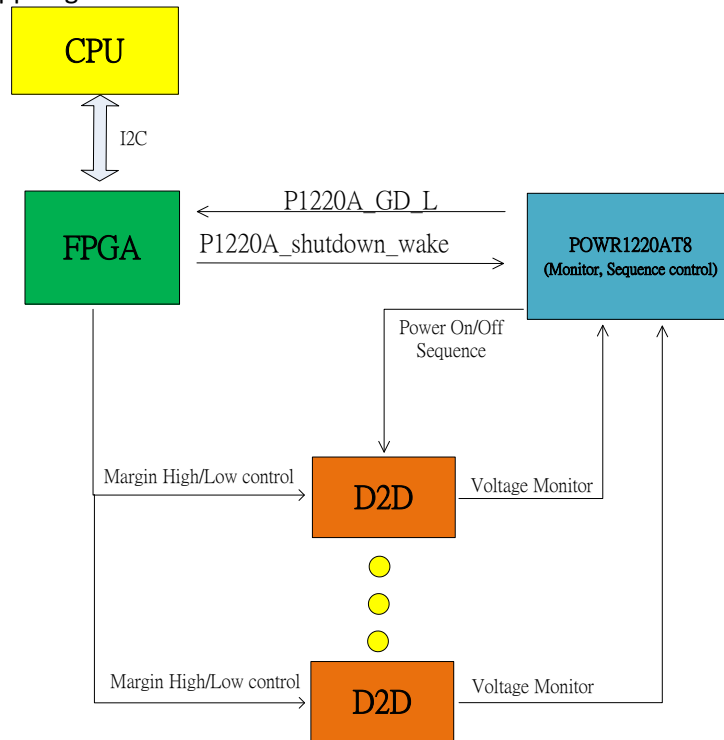


Figure 32 Main Board Power On/Off and Margin High/Low control

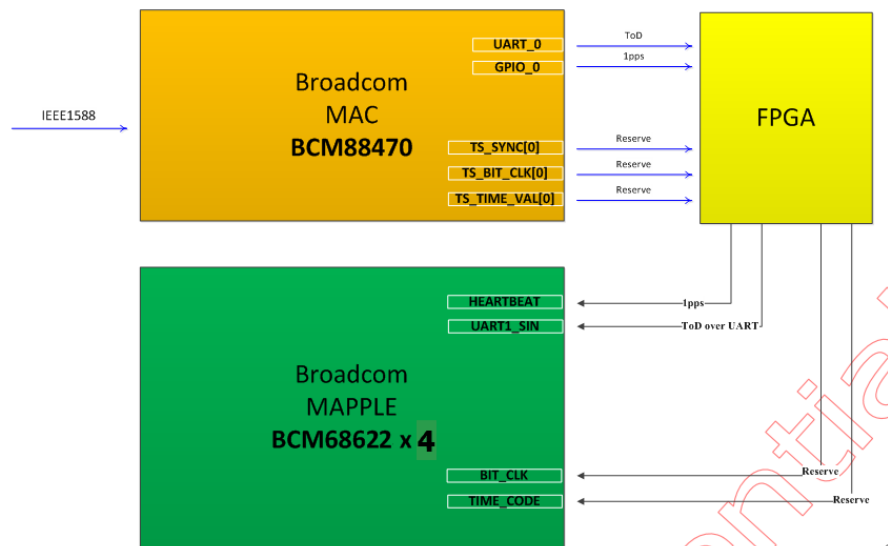


Figure 33 Broadcast ToD message from BCM88470 to Each BCM68622

2.12.2. CPLD

CPLD is at Main Board. I2C access address see Figure 13. Please see section 2.3 for detail access method.

CPLD functions as below:

1. SFP Port LED Link/Act indicates for PON Port 0 to PON Port 63.

2. QSFP28 Port LED Link/Act indicates for 100G Port 0 to Port 1.
3. SFP28 Port LED Link/Act indicates for 25G Port 0 to Port 7.
4. G-PON OLT transceiver status detect (Mode Absent, Fault, Disable, Reset...)
5. 40G/100G Optical transceiver status detect (Mode, Present, Reset...)
6. Uplink Port rate LED indicates. (40G/100G)
7. Uplink Port SERDES lane LED control that indicate which lane access to optical transceiver.
8. System LED controls. (Power Supply, Diag, FAN, LOC)

CPLD upgrade by JTAG that can through external connector or CPU, please see [Figure 30](#) for detail block diagram.

Figure 34 shows LED stream from BCM88470 to CPLD then decode by CPLD.
CPLD base on decode result to indicate each port LED status.

Figure 35 show LED stream bit define table. Detail please see CPLD spec

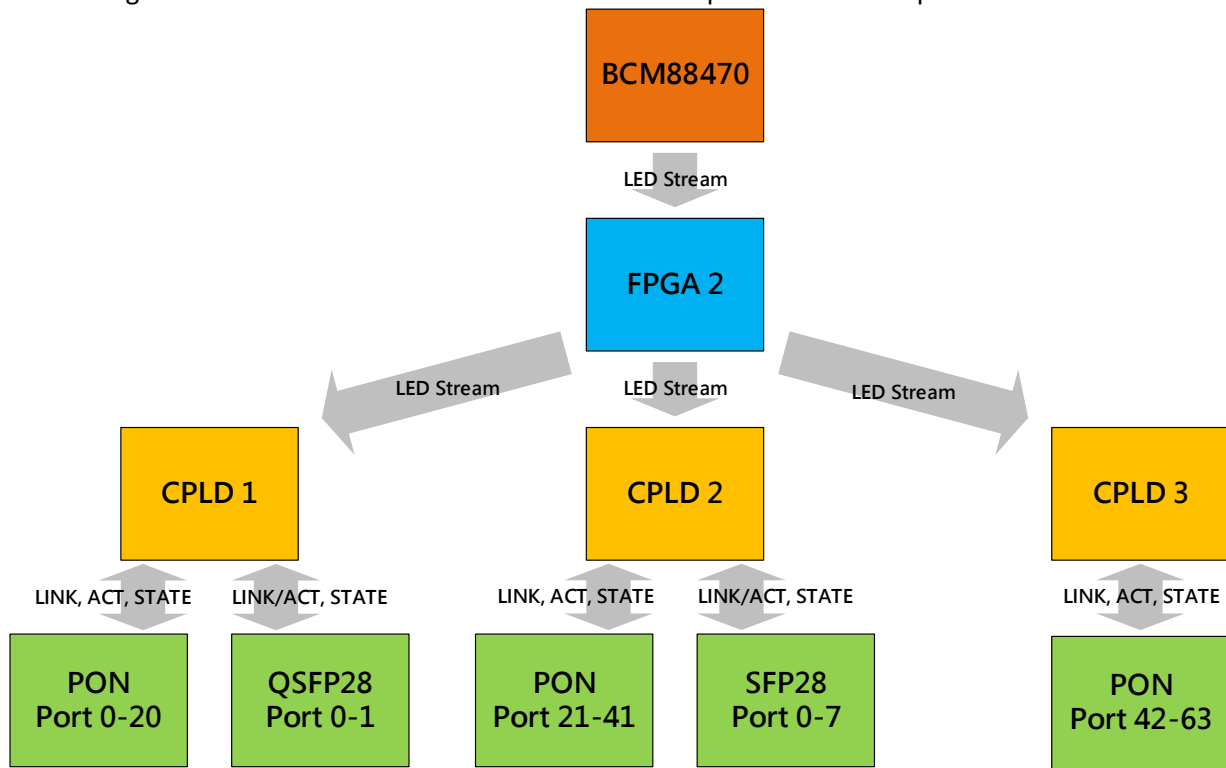


Figure 34 LED control methods

0	1	2	3	4	5	6	7	8	9	10	11
PON Port 0			PON Port 1			PON Port 2			PON Port 3		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
12	13	14	15	16	17	18	19	20	21	22	23
PON Port 4			PON Port 5			PON Port 6			PON Port 7		

LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
24	25	26	27	28	29	30	31	32	33	34	35
PON Port 8			PON Port 9			PON Port 10			PON Port 11		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
36	37	38	39	40	41	42	43	44	45	46	47
PON Port 12			PON Port 13			PON Port 14			PON Port 15		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
48	49	50	51	52	53	54	55	56	57	58	59
PON Port 16			PON Port 17			PON Port 18			PON Port 19		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
60	61	62	63	64	65	66	67	68	69	70	71
PON Port 20			PON Port 21			PON Port 22			PON Port 23		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
72	73	74	75	76	77	78	79	80	81	82	83
PON Port 24			PON Port 25			PON Port 26			PON Port 27		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
84	85	86	87	88	89	90	91	92	93	94	95
PON Port 28			PON Port 29			PON Port 30			PON Port 31		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
96	97	98	99	100	101	102	103	104	105	106	107
PON Port 32			PON Port 33			PON Port 34			PON Port 35		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
108	109	110	111	112	113	114	115	116	117	118	119
PON Port 36			PON Port 37			PON Port 38			PON Port 39		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT

120	121	122	123	124	125	126	127	128	129	130	131
PON Port 40			PON Port 41			PON Port 42			PON Port 43		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
132	133	134	135	136	137	138	139	140	141	142	143
PON Port 44			PON Port 45			PON Port 46			PON Port 47		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
144	145	146	147	148	149	150	151	152	153	154	155
PON Port 48			PON Port 49			PON Port 50			PON Port 51		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
156	157	158	159	160	161	162	163	164	165	166	167
PON Port 52			PON Port 53			PON Port 54			PON Port 55		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
168	169	170	171	172	173	174	175	176	177	178	179
PON Port 56			PON Port 57			PON Port 58			PON Port 59		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT
180	181	182	183	184	185	186	187	188	189	190	191
PON Port 60			PON Port 61			PON Port 62			PON Port 63		
LINK		ACT	LINK		ACT	LINK		ACT	LINK		ACT

Example:

Link
00 : Green steady – PON link up and 1 or more ONTs
01: Blue – port disabled
10: Red – fault detected
11: Off – No ONT in service

ACT
1: Green steady - no traffic
0: Green blinking - indicates data traffic on the PON

0	1	2	3	4	5	6	7
---	---	---	---	---	---	---	---

QSFP28 Port 0-Lane 1				QSFP28 Port 0-Lane 2			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
8	9	10	11	12	13	14	15
QSFP28 Port 0-Lane 3				QSFP28 Port 0-Lane 4			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
16	17	18	19	20	21	22	23
QSFP28 Port 1-Lane 1				QSFP28 Port 1-Lane 2			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
24	25	26	27	28	29	30	31
QSFP28 Port 1-Lane 3				QSFP28 Port 1-Lane 4			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
32	33	34	35	36	37	38	39
SFP28 Port 0				SFP28 Port 1			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
40	41	42	43	44	45	46	47
SFP28 Port 2				SFP28 Port 3			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
48	49	50	51	52	53	54	55
SFP28 Port 4				SFP28 Port 5			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	
56	57	58	59	60	61	62	63
SFP28 Port 6				SFP28 Port 7			
LINK	ACT(Blinking)	Speed		LINK	ACT(Blinking)	Speed	

Example:

LINK
1: Link Down 0: Link Up

ACT
1: No Traffic
0: Traffic

SPEED
00: Green – 100G or 4x25G break-out link up
01: Blue – 40G or 4x10G break-out link up
10: Orange – 4G or 4x1G break-out link up
11: no link

Figure 35 LED Stream bit define

2.12.3. Fan Board CPLD Register

Address	Register	R/W	Default value
0x00	Board Info	Read Only	
0x01	CPLD Version	Read Only	
0x08	Fan CPLD Reset	Read& Write	0x80
0x20	MISC_1	Read& Write	
0x28	WD_status	Read& Write	
0x29	Watchdog_Timer	Read& Write	
0x2A	Watchdog_Trigger	Read& Write	
0x80	Fan Module Present	Read Only	
0x81	Fan Module Direction	Read Only	
0x82	Interrupt Mask	Read& Write	0x00
0x83	Interrupt Status	Read Only	0x7F
0x84	LED Display (G/OFF)	Read Only	
0x85	LED Display (R/OFF)	Read Only	
0x86	Fan Module Power enable	Read& Write	0x0F
0x87	Fan Module PWM	Read& Write	0x0A
0x88	FAN CLK DEVIDER PWM	Read & Write	0x03
0x89	FAN CLK DEVIDER Teck	Read & Write	0x08
0x8A	Front Fan min Speed set	Read & Write	0x00
0x8B	Front Fan max Speed set	Read & Write	0xFF
0x8C	Rear Fan min Speed set	Read & Write	0x00
0x8D	Rear Fan max Speed set	Read & Write	0xFF
0x90	Front Fan1 Module Speed	Read Only	
0x91	Front Fan2 Module Speed	Read Only	
0x92	Front Fan3 Module Speed	Read Only	
0x93	Front Fan4 Module Speed	Read Only	

0x98	Rear Fan1 Module Speed	Read Only	
0x99	Rear Fan2 Module Speed	Read Only	
0x9A	Rear Fan3 Module Speed	Read Only	
0x9B	Rear Fan4 Module Speed	Read Only	

Table 15 Fan CPLD I/O Register Table

2.12.3.1. Offset 0x00 Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Version_ID[3:0]	R		000: R0A 001: R0B 100: R01 Others: Reserved
3:0	Board_ID[3:0]	R		00:ZZ 01: Reserved 10: Reserved 11: Reserved

2.12.3.2. Offset 0x01 CPLD Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Released Bit	R		0= not released 1= Released version after PVT
6:4	Reserved	R		
3:0	CPLD_ver[3:0]	R		CPLD version

2.12.3.3. Offset 0x08 Fan CPLD Reset (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reset_CPLD	R/W	1	1: CPLD is placed in normal operation state. (Default) 0: CPLD is placed in reset state.
6:0	Reserved	N/A	N/A	

*The register will return to default automatically after write to Low

2.12.3.4. Offset 0x20 MISC_1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved	N/A	N/A	
1	JTAG_select (CPLD_UPD_DISABLE)	R/W	1	0 = Main Board Program 1 = JTAG Program (Default)
0	Clock_select	R/W	0	0 = CPLD internal OSC 24.7MHz (Default) 1 = External 25MHz

2.12.3.5. Offset 0x28 Watchdog Enable/Status (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved	N/A	N/A	
1	WDT_Timer_update	R/W	0	0 = level 1(Default) 1 =Write Level1_Timer_Value (0x29) into WDT counter
0	Watchdog_EN	R/W	0	0 = Disable(Default) 1 = Enable

*When WDT timeout, the FAN will full speed running.

2.12.3.6. Offset 0x29 Watchdog Timer (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Level1_Timer_Value	R/W	1111_1111	# of counting value Default value: 0xFF Internal of each counting : 25ms W: Set the timer value R: Read the real timer value

2.12.3.7. Offset 0x2A Watchdog Trigger (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved	N/A	N/A	
1	WDT_timeout_full_run	R		WDT time out Flag
0	Watchdog_Trigger	R/W	0	1: Trigger will set the watchdog timer to default value. 0: No Trigger.

*The register will return to default automatically after write to H.

2.12.3.8. Offset 0x80 Fan Module Present (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved	N/A	N/A	
3	Fan_present4	R	1	1: Fan4 isn't inserted 0: Fan4 is inserted
2	Fan_present3	R	1	1: Fan3 isn't inserted 0: Fan3 is inserted
1	Fan_present2	R	1	1: Fan2 isn't inserted 0: Fan2 is inserted
0	Fan_present1	R	1	1: Fan1 isn't inserted 0: Fan1 is inserted

2.12.3.9. Offset 0x81 Fan Module Direction (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved	N/A	N/A	
3	Fan_DIR4	R		1: The air flow of Fan4 is "back to front" 0: The air flow of Fan4 is "front to back"
2	Fan_DIR3	R		1: The air flow of Fan3 is "back to front" 0: The air flow of Fan3 is "front to back"
1	Fan_DIR2	R		1: The air flow of Fan2 is "back to front" 0: The air flow of Fan2 is "front to back"
0	Fan_DIR1	R		1: The air flow of Fan1 is "back to front" 0: The air flow of Fan1 is "front to back"

2.12.3.10. Offset 0x82 Interrupt Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	TEMP_SENSOR_INT_mask_2	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	TEMP_SENSOR_INT_mask_1	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5:4	Reserved	N/A	N/A	
3	Fan_int_mask_4	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	Fan_int_mask_3	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	Fan_int_mask_2	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	Fan_int_mask_1	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

*The default will be set H when Engineer sample.

2.12.3.11. Offset 0x83 Interrupt Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7	TEMP_SENSOR_INT_2	R	1	1: No interrupt 0: There is INTR to CPU
6	TEMP_SENSOR_INT_1	R	1	1: No interrupt 0: There is INTR to CPU
5:4	Reserved	N/A	N/A	
3	Fan_interrupt	R	1	1: No interrupt 0: There is INTR to CPU
2	Fan_interrupt	R	1	1: No interrupt 0: There is INTR to CPU
1	Fan_interrupt	R	1	1: No interrupt 0: There is INTR to CPU
0	Fan_interrupt	R	1	1: No interrupt 0: There is INTR to CPU

*CPLD will inform CPU by fan interrupt signal if there has fan fail occur, temp sensor alert.

2.12.3.12. Offset 0x84 LED Display (G/OFF) (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Reserved			
3	FAN4_LED_G	R		1: Fan4 _LED is Green 0: off
2	FAN3_LED_G	R		1: Fan3 _LED is Green 0: off
1	FAN2_LED_G	R		1: Fan2 _LED is Green 0: off
0	FAN1_LED_G	R		1: Fan1 _LED is Green 0: off

2.12.3.13. Offset 0x86 Fan Module Power enable (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Reserved			
3	FAN4_LED_R	R		1: Fan4 _LED is Red 0: off
2	FAN3_LED_R	R		1: Fan3 _LED is Red 0: off
1	FAN2_LED_R	R		1: Fan2 _LED is Red 0: off
0	FAN1_LED_R	R		1: Fan1 _LED is Red 0: off

2.12.3.14. Offset 0x86 Fan Module Power enable (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved	N/A	N/A	
3	EN_FAN4	R/W	1	1: Enable the fan Power 0: Disable the fan power
2	EN_FAN3	R/W	1	1: Enable the fan Power 0: Disable the fan power
1	EN_FAN2	R/W	1	1: Enable the fan Power 0: Disable the fan power
0	EN_FAN1	R/W	1	1: Enable the fan Power 0: Disable the fan power

2.12.3.15. Offset 0x87 Fan Module PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved	N/A	N/A	
3	Fan_DIR4	R		1: The air flow of Fan4 is "back to front" 0: The air flow of Fan4 is "front to back"
2	Fan_DIR3	R		1: The air flow of Fan3 is "back to front" 0: The air flow of Fan3 is "front to back"
1	Fan_DIR2	R		1: The air flow of Fan2 is "back to front" 0: The air flow of Fan2 is "front to back"
0	Fan_DIR1	R		1: The air flow of Fan1 is "back to front" 0: The air flow of Fan1 is "front to back"
3:0	Fan PWM [3:0]	R/W	0101	0000 : 0 % duty cycle 0001 : 17.6 % duty cycle 0010 : 23.6 % duty cycle 0011 : 29.4 % duty cycle 0100 : 35.3 % duty cycle 0101 : 41.2 % duty cycle (default) 0110 : 47.0 % duty cycle 0111 : 52.9 % duty cycle 1000 : 58.8 % duty cycle 1001 : 64.7 % duty cycle 1010 : 70.6 % duty cycle 1011 : 76.5 % duty cycle 1100 : 82.3 % duty cycle 1101 : 88.2 % duty cycle 1110 : 94.1 % duty cycle 1111 : 100 % duty cycle

2.12.3.16. Offset 0x88 FAN CLK DEVIDER PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reverse			
4:0	CLK_Dediver_PWM_REG[7:0]	R/W	0101	91.912 K Hz

RTL : base 25MHz => clk_cnt[31:0]

Use clk_cnt[X] as clock base to generate 16 level duty cycle PWM

CLK_Dedive_PWM_REG[2:0]	clk_div	tachometer sample frequency (Hz)
0000	clk_cnt[0]	735.3 K
0001	clk_cnt[1]	367.6 K
0010	clk_cnt[2]	183.8 K
0011	clk_cnt[3]	91.9 K (default)
0100	clk_cnt[4]	46.0 K
0101	clk_cnt[5]	23.0 K
0110	clk_cnt[6]	11.5 K
0111	clk_cnt[7]	5.7 K
1000	clk_cnt[8]	2.9 K
1001	clk_cnt[9]	1.4 K
1010	clk_cnt[10]	718
1011	clk_cnt[11]	359.0
1100	clk_cnt[12]	179.5
1101	clk_cnt[13]	89.8
1110	clk_cnt[14]	44.9
1111	clk_cnt[15]	22.4

2.12.3.17. Offset 0x89 FAN CLK DEVIDER Teck (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reverse			
4:0	CLK_Dedive_teck_REG[7:0]	R/W	08	

CLK_Dedive_teck_REG[3:0]	tachometer sample frequency (Hz)
0000	12.5 M
0001	6.25 M
0010	3.125 M
0011	1.563 M
0100	781.25 K
0101	390 K
0110	195.313 K
0111	97.656 K
1000	48.84 K (default)
1001	24.414 K
1010	12.207 K
1011	6.104 K
1100	3.052 K
1101	1.526 K
1110	763.94
1111	381.472

2.12.3.18. Offset 0x8A Front Fan min Speed set (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Front_min_speed_set	R/W	00	1 ~ 255: the number

2.12.3.19. Offset 0x8B Front Fan max Speed set (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Front_max_speed_set	R/W	FF	1 ~ 255: the number

2.12.3.20. Offset 0x8C Rear Fan min Speed set (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Front_min_speed_set	R/W	00	1 ~ 255: the number

2.12.3.21. Offset 0x8D Rear Fan max Speed set (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:0	Front_max_speed_set	R/W	FF	1 ~ 255: the number

2.12.3.22. Offset 0x90 Front Fan1 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Fan1_SENSOR	R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.23. Offset 0x91 Front Fan2 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Fan2_SENSOR	R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.24. Offset 0x92 Front Fan3 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Fan3_SENSOR	R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.25. Offset 0x93 Front Fan4 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Fan4_SENSOR	R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.26. Offset 0x98 Rear Fan1 Module Speed (Read Only)

Bit	Name		R/W	Reset Value	Description
7:0	FAN1R_SENSOR		R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.27. Offset 0x99 Rear Fan2 Module Speed (Read Only)

Bit	Name		R/W	Reset Value	Description
7:0	FAN2R_SENSOR		R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.28. Offset 0x9A Rear Fan3 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN3R_SENSOR	R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.3.29. Offset 0x9B Rear Fan4 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN4R_SENSOR	R		0: Fan failed 1 ~ 255: the number of ½ rotations in 300ms

2.12.4. CPU Board of CPLD Register

Address	Register	R/W	Default value
0x00	Board Info	Read Only	0x02
0x01	CPLD version	Read Only	0x11
0x02	Watch DOG Status_1	Read / Write	
0x03	Watch DOG Status_2	Read / Write	
0x04	System Reset	Read / Write	0x01
0x24	Last Reset Reason	Read Only	

Table 16 CPU Board of CPLD I/O Register Summary

2.12.4.1. Offset 0x00 Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved	NA	NA	
0	PCB version	R	0x2	0x2 for R02

2.12.4.2. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x11	CPLD version

2.12.4.3. Offset 0x02 Watch Dog Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7	OS_done	R/W		1: Had enter into OS 0: not enter into OS Note: OS needs set “1”, this bit will auto return to 0 when system reset or power cycle.
6	Reset_log_clear	R/W		For 0x24 clear 1: clear 0x24 0: Normal
5	Reserved	NA	NA	
4	SPI_CS_SELECT	R		The state of flash 1: Boot from CI flash 0: Boot from KGI flash
3	Last_time_ SPI_CS_SELECT			The state of flash 1: Boot from CI flash 0: Boot from KGI flash
2:0	Reserved	NA	NA	

2.12.4.4. Offset 0x03 Watch Dog Status_2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved	NA	NA	
4	Watch dog enable	R/W	0	Function: Enable / Disable Watchdog function 1: Enable watch dog function 0: Disable watch dog function
3	Update_BOOT_DEV_SEL	R/W	0	1: Update_BOOT_DEV_SEL 0: None
2	BOOT_DEV_SEL	R/W	1	Function: Bios boot flash select 1: Boot from CI flash 0: Boot from KGI flash
1	WATCHDOG_Trigger	R/W	1	Function: Negative edge trigger for WDT Need set L to H in 300 sec WDT, no autoreturn (H-L-H)
0	test_mode	R/W	0	Function: For reduce the time for WDT test 1: Reduce time (60 sec) 0: Normal run (300 sec)

2.12.4.5. Offset 0x04 System Reset (Read& Write)

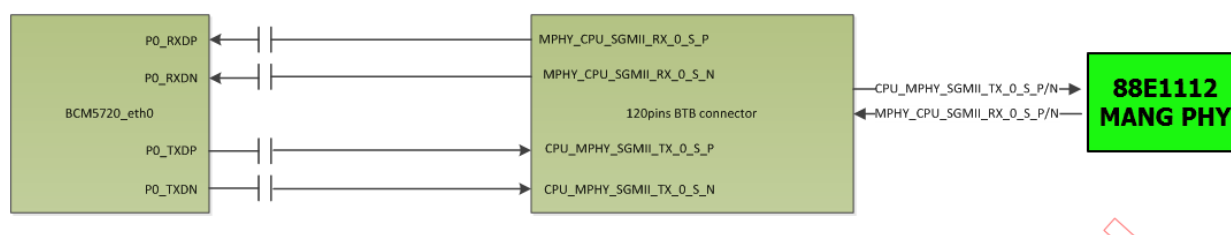
Bit	Name	R/W	Reset Value	Description
7:1	Reserved	NA	NA	
0	Soft reset	R/W	1	0: the system was reset by software

				1: Normal
--	--	--	--	-----------

2.12.4.6. Offset 0x24 Last Reset Register (Read)

Bit	Name	R/W	Reset Value	Description
7	OS_done_log	R		When 1: It has entry OS before When 0: It has not entry OS before
6	POWER_ON_log	R		When 1: It has power ON before When 0: It has no power ON before
5	Reserved	NA	NA	
4	PSHBTN_SYS_RESET_N	R		When 1: Last reset caused by PSHBTN_SYS_RESET_N When 0: Last reset not caused by PSHBTN_SYS_RESET_N
3	Reserved	NA	NA	
2	Manu_RST	R		When 1: Last reset caused by Manu_RST on reset When 0: Last reset not caused by Manu_RST on reset
1	Soft reset_log	R		Soft reset log 0x04[0] When 1: Last reset caused by Soft reset on reset When 0: Last reset not caused by Soft reset on reset
0	CPU_WDT_log	R		When 1: Last reset caused by WDT on reset When 0: Last reset not caused by WDT on reset

2.13. SGMII

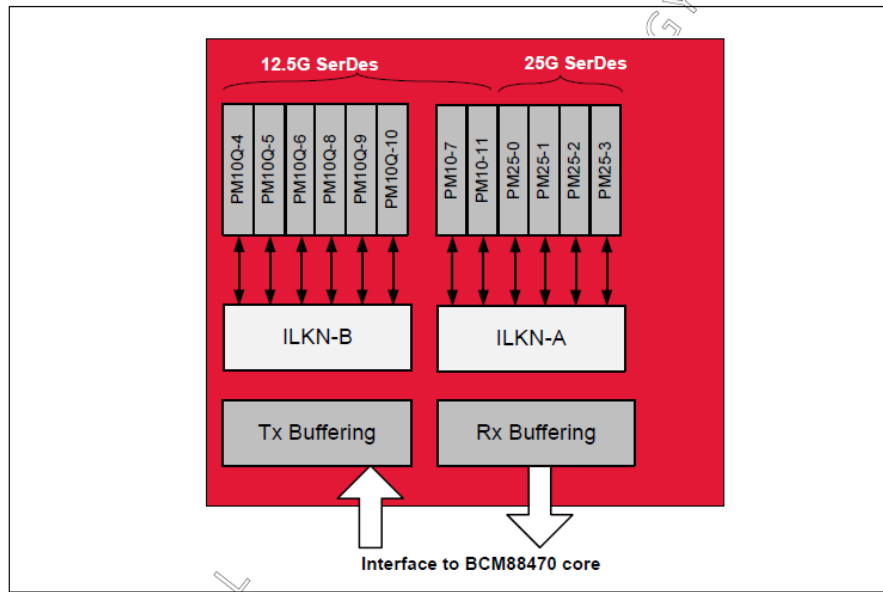


2.14. NIF/NIFe SerDes

Below shows the BCM88470 Network Interface block diagram and NIF SerDes Interface Mapping. PM25-0 to PM25-3 is running at 40G/100G per port and design for four of uplink port that connects to QSFP connector. Other NIFe SerDes is configuring as 10GbE per lane that connect to eight of BCM68622 XFI port.

For NIF/NIFe Port mapping in our design, please refer to section 1.4

Figure 6: BCM88470 Network Interface Block Diagram



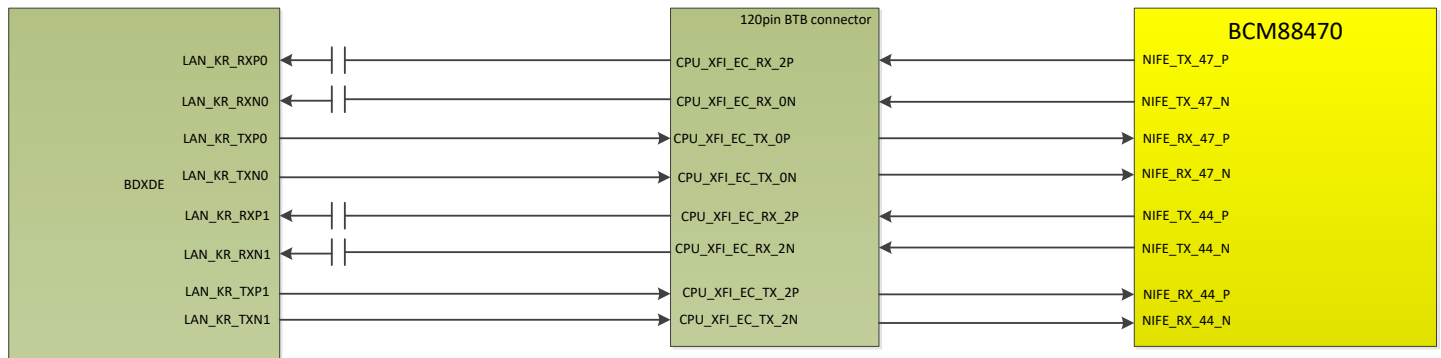
2.15. 10GBASE-KR

Section 3.15.1 introduces 10GBASE-KR between CPU board and Main Board.

2.15.1. Intel CPU and BCM88470 10GBASE-KR

Below show 10GBASE-KR block diagram and mapping information. 10GBASE-KR connect between Intel BDx-DE CPU to BCM88470 through 120 pin B2B connector.

CPU side through KR interface, BCM88470 through NIFE interface and run at 10GBASE-KR mode.



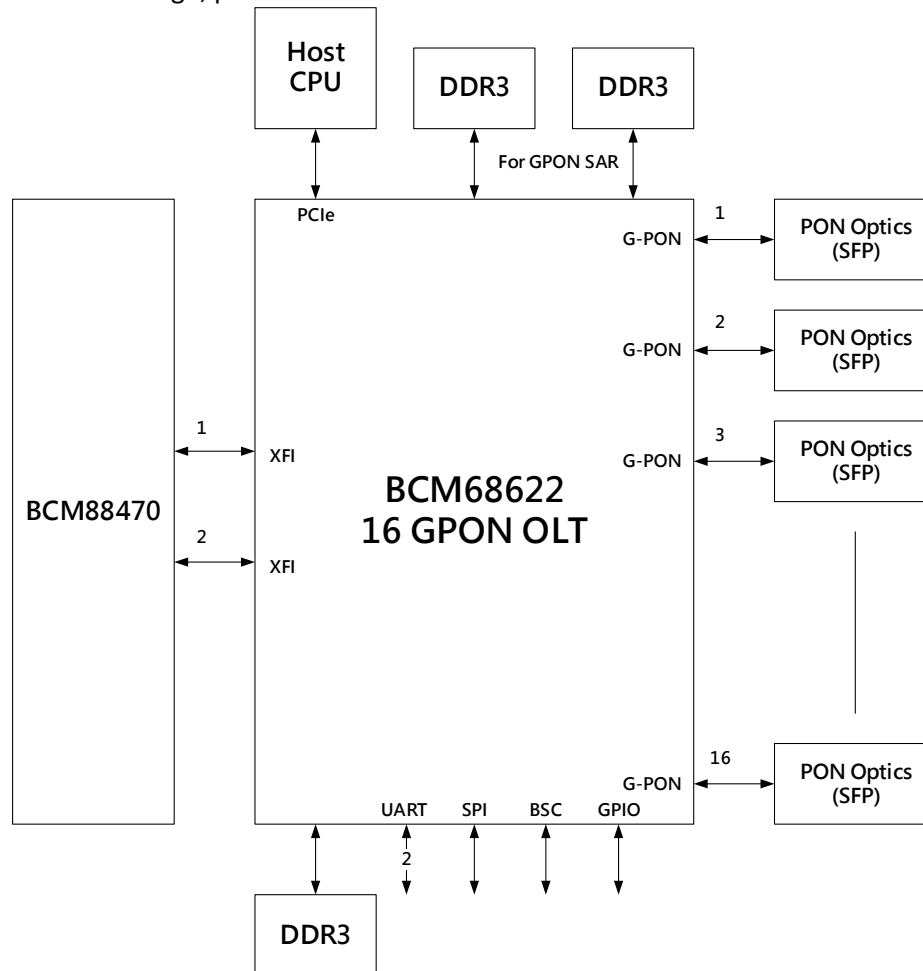
MAC BCM88470			Device		
PM10-11	NIF_TX[44]_P/N		CPU	LAN_KR_RXP1/N1	
	NIF_RX[44]_P/N		CPU	LAN_KR_TXP1/N1	
PM10-11	NIF_TX[47]_P/N		CPU	LAN_KR_RXP0/N0	
	NIF_RX[47]_P/N		CPU	LAN_KR_TXP0/N0	

2.16. XFI

Section 3.16.1 introduces XFI between BCM88470 (QAX) to BCM68622 (Maple)

2.16.1. BCM88470 and BCM68622 XFI

Below show simply block diagram for BCM68622 and XFI connect methods. Each BCM68622 support 16 of G-PON port. We connect XFI interface to BCM88470 NIF interface. For detail mapping information in our design, please refer Table 4 in section 2.4



3. Power Consumption

Power Consumption Estimation Table				
Current(mA)	Voltage(V)	(W)/device	Quantity	Total(W)
Current(mA)				
BCM68622 (U225, U170, U171, U172)		12.5716	4	50.2864
BCM88470 (U84)		57.4156	1	57.4156
DDR3-1600 (U91, U92, U93, U95, U96, U98, U101, U102, U103, U105, U108, U109, U110, U111, U112, U117, U118, U119, U121, U122, U123, U124, U125, U126, U127, U128, U129, U130, U131, U132, U139, U140, U141, U142, U143, U146, U147, U148, U149, U150)		0.6	20	12
DDR4-3200 (U2, U3, U4, U5, U6, U7)		1.3433325	6	8.059995
DDR3_VTT075 (For All of DDR3 terminal resistor)		1.096875	4	4.3875
DDR4_VTT060 (For All of DDR4 terminal resistor)		0.756	1	0.756
QSFP transceiver (CONN41, CONN42, CONN43, CONN44)		5.94	2	11.88
GPON OLT transceiver (CONN7, CONN8 , CONN9, CONN11, CONN12, CONN13, CONN14, CONN15, CONN16, CONN17, CONN20, CONN21, CONN30, CONN33, CONN39, CONN40)		1.65	64	105.6
SFP28 25G transceiver		1.65	8	13.2
SFP transceiver		1.65	1	1.65
88E1112 (U83)		1.4689	1	1.4689
89H24NT24G2 (PCIE switch) (U106)		5.6855	1	5.6855
CPLD (U104, U120)		2.01	3	6.03
FPGA		5.845	1	5.845
FPGA for PON LED		8.0612	1	8.0612
LED		16.5	1	16.5

Pin Number	Name	I/O	Active	Pin Length
P1&P2(Bottom)	+12V	I/O	Analog	Standard
P3&P4(Top)	RTN	I/O	Analog	Standard
S1	+12V SENSE	I	Analog	Standard
S2	+12V RTN SENSE	O	Analog	Standard
S3	12V I-Share	I/O	Analog	Standard
S4	SMB_ALERT [#]	O	Digital	Standard
S5	SDA	I/O	Digital	Standard
S6	SCL	I/O	Digital	Standard
S7	PS_KILL [#]	I	Low	Standard
S8	PSON [#]	I	Low	Short
S9	PWOK	O	High	Standard
S10	A1	I	Digital	Standard
S11	+5VSB	I/O	Analog	Standard
S12	+5VSB	I/O	Analog	Standard
S13	PDB_FAULT	I	Digital	Standard
S14	Present [#]	O	Low	Standard
S15	A0	I	Digital	Standard
S16	AC_OK	I	Analog	Standard
S17	N/A	O	Analog	Standard
S18	N/A	I	Low	Standard
S19	N/A	I	High	Standard
S20	N/A	-	-	Standard
S21	N/A	-	-	Standard
S22	A2	I	Digital	Standard
S23	+5VSB	I/O	Analog	Standard
S24	+5VSB	I/O	Analog	Standard

4.2. Dimension

Nominal Dimensions

Height: 40.2mm

Width: 50.5mm

Depth: 300mm

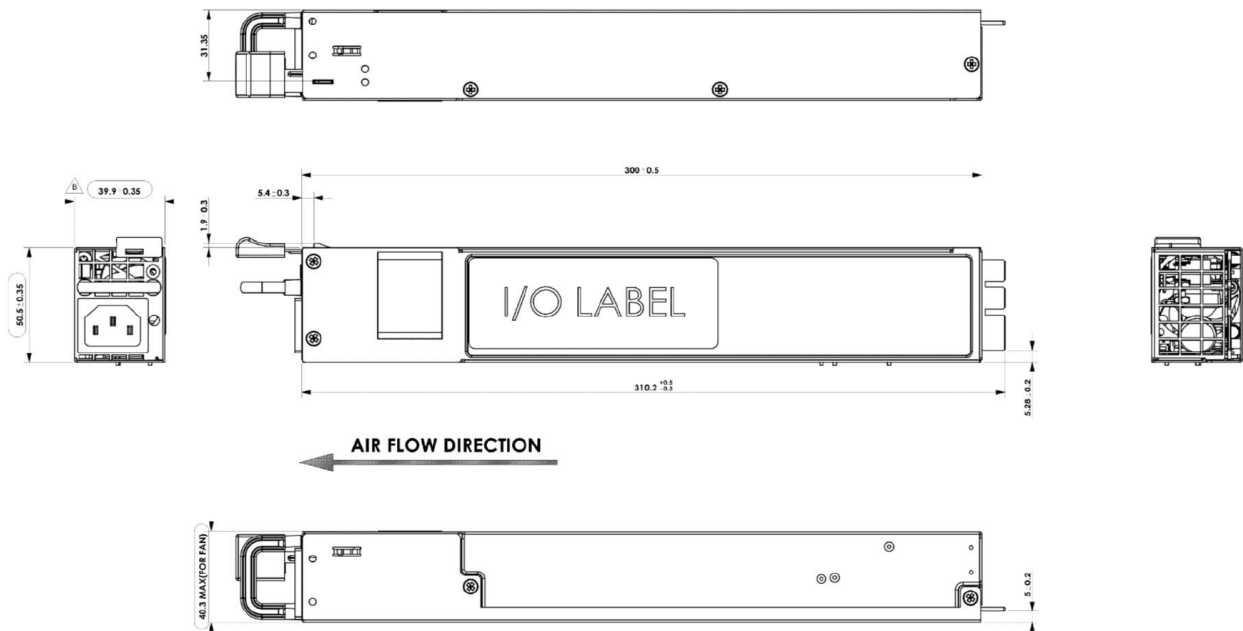


Figure 36 PSU Dimension

4.3. Efficiency

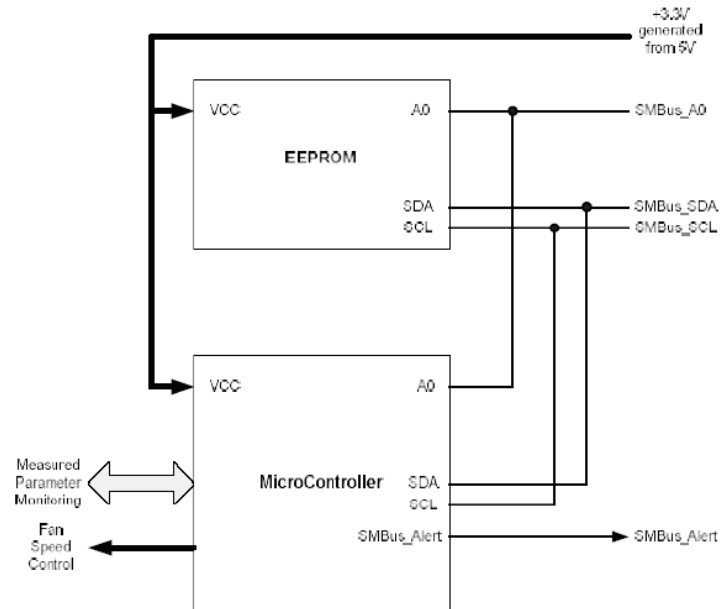
The Efficiency should meet at least 80Plus Platinum rating, specified in the below table. The efficiency test condition should be 230VAC and with external fan power source or deduction of the power consumed by the fan at specified loading, according to 80Plus efficiency measurement specifications.

Load	20% Load	50% Load	100% Load
230V AC Input	90 %	94 %	91 %

4.4. Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the 5Vsb output on the system side of the Oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2 or later. It shall be located at the address set by the A0, A1 pins. Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features.

Power Supply MicroController and EEPROM



4.4.1. PMBus™ Monitoring Interface

The Power Supply shall provide a monitoring interface to the system using a serial interface called the System Management Bus (SMBus) which is based on I2C. Devices should be compatible with both SMBus 2.0 “high power” and I2C Vdd based power and drive. This bus may operate within the power supply at 5V (Powered from 5V). Pull ups for the bus shall be located on the system motherboard.

This shall provide power monitoring, failure conditions, warning conditions and FRU data. Two pins have been reserved on the connector to provide this interface. One pin is the Serial Clock (SCL). The second pin is used for Serial Data/Address (SDA). Both pins are bi-directional and are used to form a serial I2C Bus. The protocol bit ordering shall conform to I2C Standard. The IC's connected to this bus within the power supply shall be selected by address bits A0. See below section for addresses.

The IC's in the power supply interfaced to the SMBus shall be powered by the system side of the 5V bus (after OR'ing diodes) to allow monitor operation of the power supply even when it is off. No pull up resistors shall be inside the power supply on SDA and SCL. Pull up resistors shall be located outside the power supply.

The interface shall support the SMBus Alert signal (SMB_ALERT) as an interrupt to the system indicating the power supply should be checked for status and warnings.

SMB_ALERT shall be an open collector / open drain output from the power supply with pull

up to +5V on the system side of the interface.

It is recommended that the power supply operate at the full 100Kbps SMBus speed without using clock stretching to slow down the bus.

4.4.2. Device Address Location

The Power Supply device address locations are shown below. Two signal to set the address location of the PS once it is installed into the system:

Address A1/A0	FRU Device	PMBUS Device
Low/Low	A0h	B0h
Low/High	A2h	B2h
High/Low	A4h	B4h
High/High	A6h	B6h

SMBus Status and Control registers

4.5. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose. All Sensors shall continue to provide real time data as long as the PSMC device is powered. This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Sensor	Description
Vinput	Input Voltage
Iinput	Input Current
Pinput	Input Power
Voutput_main	Output Voltage main output
Ioutput_main	Output Current main output
Poutput_main	Output Power main output
Voutput_aux	Output Voltage auxiliary output
Ioutput_aux	Output Current auxiliary output
Poutput_aux	Output Power auxiliary output
Tcomp(TBD)	Component Temperature
Tenv	Environmental Temperature
RPMFan	Fan Speed reading
PDBfail	PDB fail protection

PSMC Sensor list

5. PCB

5.1. Stackup



Date: 2019/1/29 14:25

p/N: DFM-12-181219S-acc

Layers: LAYER 12

Tg: Material: TU-872LK

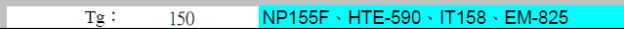
Layer Name	Plane Description		Remain Copper (%)	reduce after pressed	finish Thickness	DK 1GHz	DF 1GHz	DK 5GHz	DF 5GHz	DK 10GHz	DF 10GHz	Roughness (R2)
	solder mask				0.50							
Layer 1	Signal	1/2oz +Plating			1.43							4.2
	PREPREG				2.38	3.46	0.0087	3.29	0.0089	3.27	0.0092	
Layer 2	POW/GND	1/2oz	80	0.12	0.60							3
	CORE				3.00	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 3	Signal	1/2oz	60	0.24	0.60							3
	PREPREG				6.13	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 4	POW/GND	1/2oz	80	0.12	0.60							3
	CORE				3.00	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 5	Signal	1/2oz	60	0.24	0.60							3
	PREPREG				5.59	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 6	POW/GND	2oz	80	0.52	2.60							3
	CORE				21.09	3.85	0.0080	3.71	0.0084	3.67	0.0089	
Layer 7	POW/GND	2oz	80	0.52	2.60							3
	PREPREG				5.59	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 8	Signal	1/2oz	60	0.24	0.60							3
	CORE				3.00	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 9	POW/GND	1/2oz	80	0.12	0.60							3
	PREPREG				6.13	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 10	Signal	1/2oz	60	0.24	0.60							3
	CORE				3.00	3.65	0.0084	3.50	0.0086	3.47	0.0090	
Layer 11	POW/GND	1/2oz	80	0.12	0.60							3
	PREPREG				2.38	3.46	0.0087	3.29	0.0089	3.27	0.0092	
Layer 12	Signal	1/2oz +Plating			1.43							4.2
	solder mask				0.50							
Total Thickness=			1.91	2.79	75.07							

1. 疊構與阻抗均為理論試算值，成品以符合客戶規格為製作原則
All value of impedance and stack up are in simulate calculated, the finished board should be meet customer requirement.
2. 為符合阻抗要求，製作時會依廠內製程參數作微調，成品需符合IPC規範與客戶要求
In order to meet impedance control, this design will be fine tune by process needed during the PCB fabrication and the finished should be meet IPC specification and customer requirement.
3. 若Gerber內並無阻抗表所指定的線寬設計，製作時將直接取消該阻值控制要求
If gerber file without assignment trace design, we will cancel which impedance control directly when PCB production.
4. 小於50Ω的阻抗公差規格不足±5Ω者，依廠內製程能力設定該阻抗公差為±5Ω
When impedance requirement was smaller than 50Ω and which tolerance less than ±5Ω, according to our capability the tolerance for it will be default as ±5Ω.

Figure 37 CPU board PCB Stackup

Board thickness :		3.0mm											
☐ Y / ☒ N Gold Finger													
ACCL Stack up TU883(VLP)													
Layer Type		Layer Material	DK(1G)	DK(5G)	DK(10G)	DK(12.5G)	DK(20G)	DF(1G)	DF(5G)	DF(10G)	DF(12.5G)	DF(20G)	Thickness(mil)
L1 SM		-	4.2	No Data	No Data	No Data	No Data	0.026	0.027	No Data	No Data	No Data	0.7
L1 TOP	S	Cu+plating											1.6
		1078	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	2.76
L2	G	1.0 oz											1.2
		0.003"[(1078*1)1/2	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	3
L3	G	2.0 oz											2.4
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.28
L4	G	1.0 oz											1.2
		0.006"[(1078*2)1/H	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	6
L5	S	0.5 oz											0.6
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.46
L6	G	1.0 oz											1.2
		0.006"[(1078*2)1/H	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	6
L7	S	0.5 oz											0.6
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.46
L8	G	1.0 oz											1.2
		0.006"[(1078*2)1/H	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	6
L9	S	0.5 oz											0.6
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.46
L10	G	1.0 oz											1.2
		0.003"[(1078*1)1/1	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	3
L11	G	1.0 oz											1.2
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.46
L12	S	0.5 oz											0.6
		0.006"[(1078*2)H/1	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	6
L13	G	1.0 oz											1.2
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.46
L14	S	0.5 oz											0.6
		0.006"[(1078*2)H/1	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	6
L15	G	1.0 oz											1.2
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.46
L16	S	0.5 oz											0.6
		0.006"[(1078*2)H/1	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	6
L17	G	1.0 oz											1.2
		1078*2	3.12	3.11	3.09	3.08	3.06	0.0029	0.0036	0.0045	0.0046	0.005	5.28
L18	G	2.0 oz											2.4
		0.003"[(1078*1)2/1	3.3	3.28	3.27	3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	3
L19	G	1.0 oz											1.2
		1078	3.3	3.28		3.26	3.24	0.003	0.0037	0.0046	0.0047	0.0051	2.76
L20 BOT	S	Cu+plating											1.6
L20SM		-	4.2	No Data	No Data	No Data	No Data	0.026	0.027	No Data	No Data	No Data	0.7
													118.84

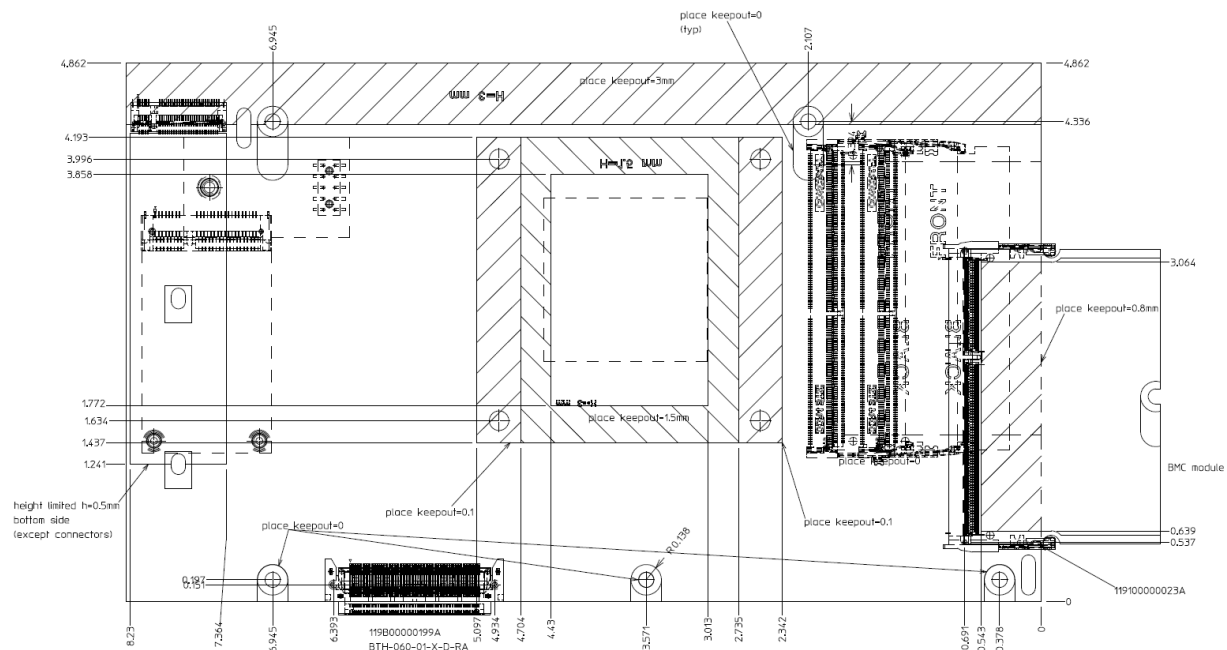
Figure 38 Mainboard board PCB Stackup



Layer Name	Plane Description	Remain Copper (%)	reduce after pressed	Material Thickness	finish Thickness	tolerance	成本	Er	Single-end Impedance	50ohm Width	differential Impedance	100ohm Width/Space	Ref.
	solder mask			0.5									
Layer1	Signal			1.4					50	8	100	5.5/5	L2
	PREPREG			4.6	4.425	+/-1	1.16	3.85					
Layer2	POW/GND	86%	0.175	1.25									
	CORE			76.34	76.34	+/-10%	25.48	4					
Layer3	POW/GND	86%	0.175	1.25									
	PREPREG			4.6	4.425	+/-1	1.16	3.85					
LAYER 4	Signal			1.4					50	8	100	5.5/5	L3
	solder mask			0.5									
Total Thickness= 2.32 mm			0.35	91.84	91.49		27.8						

Figure 39 Fan board PCB Stackup

5.2. Dimension



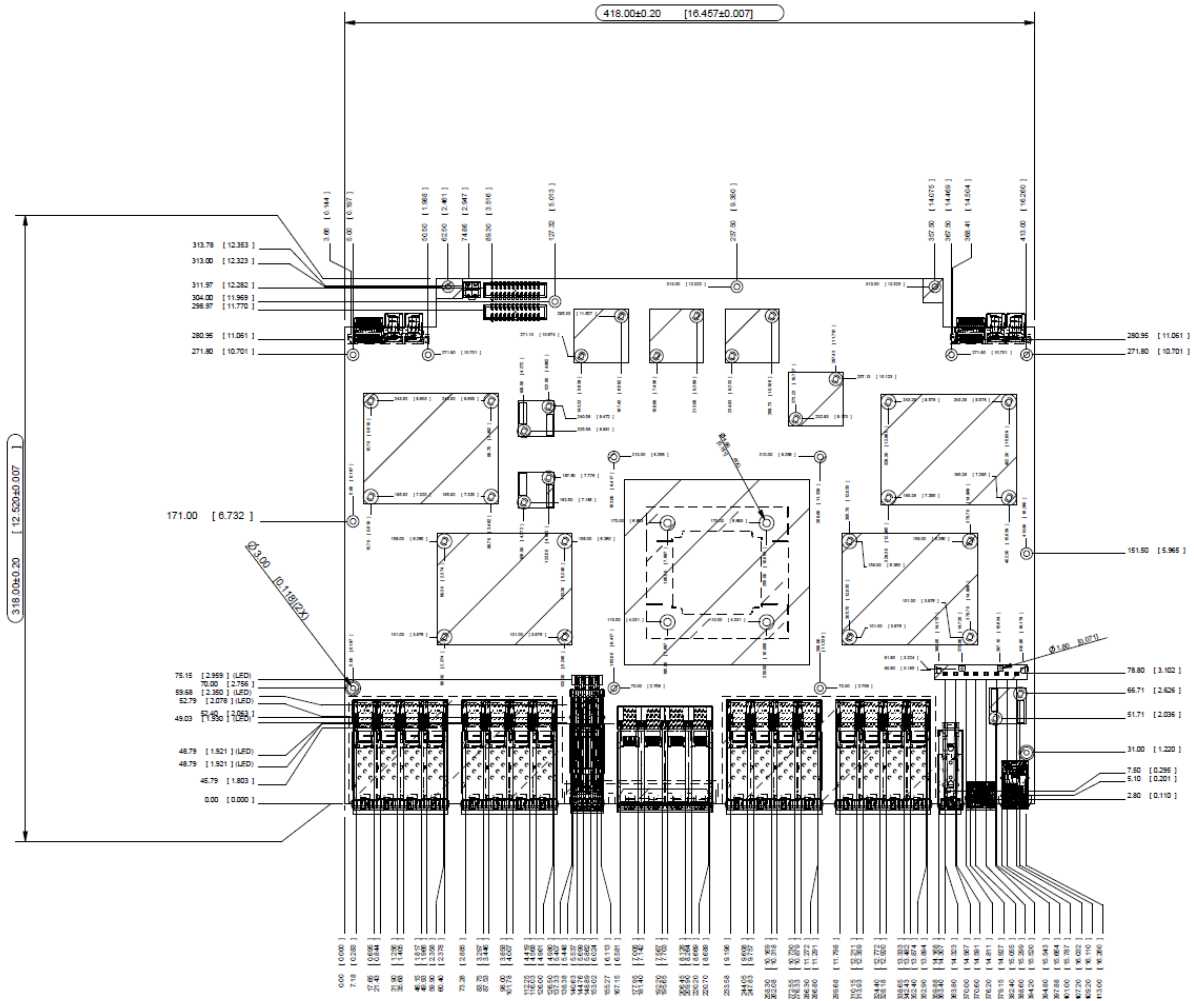


Figure 41 Mainboard PCB Dimension

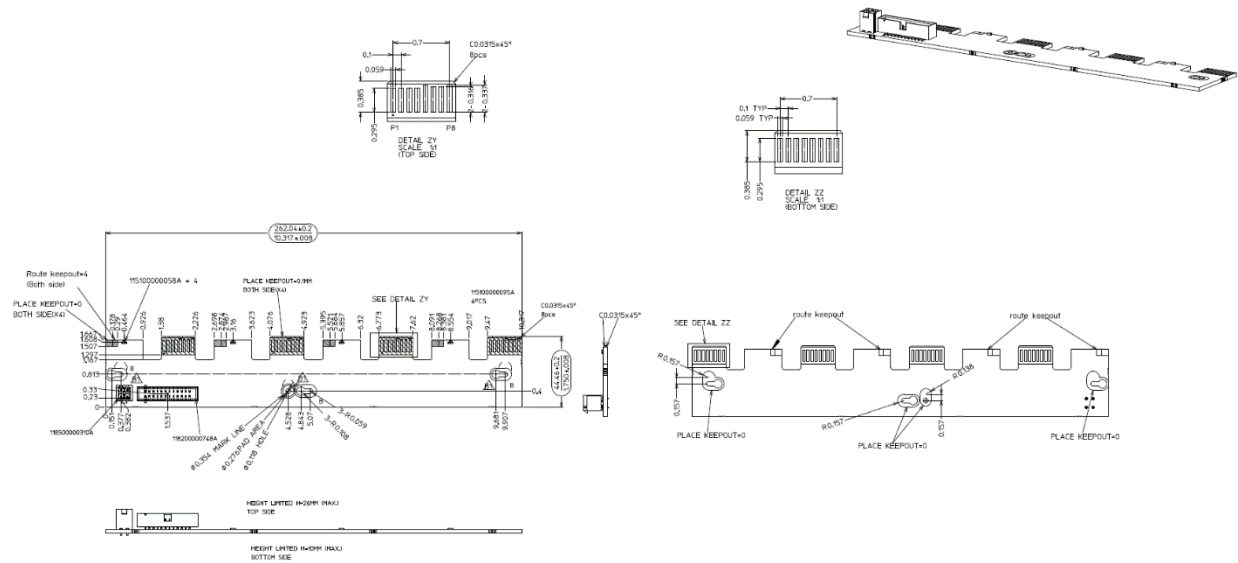


Figure 42 FAN board PCB Dimension

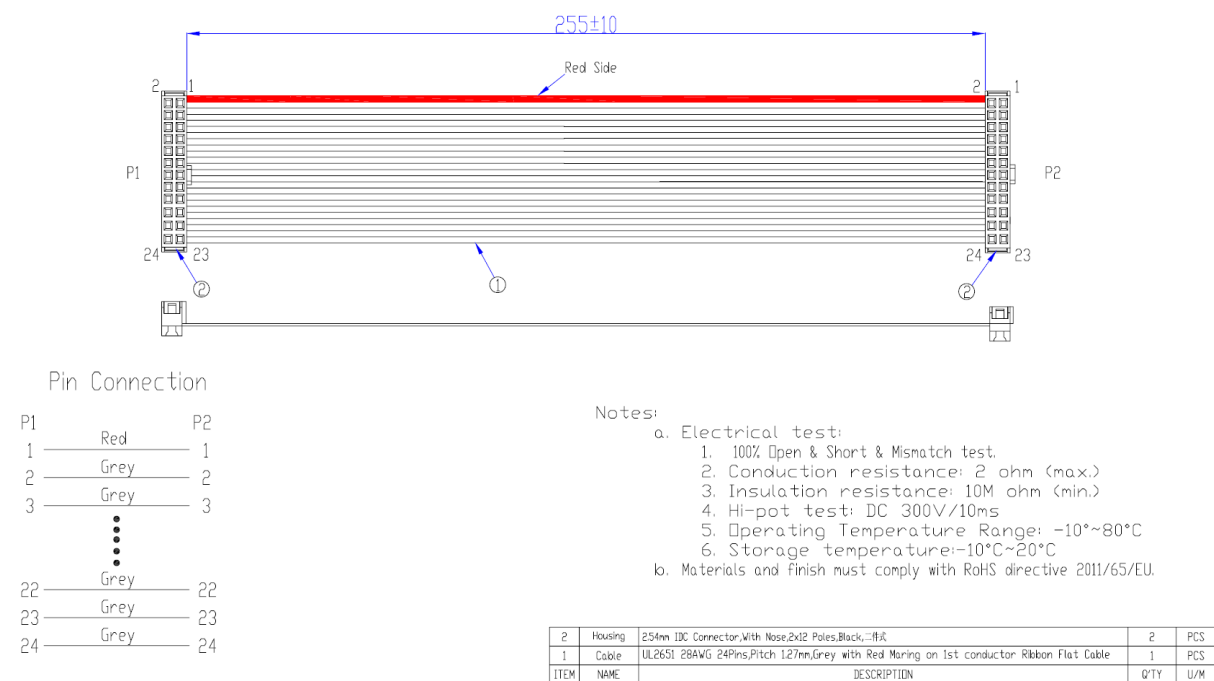


Figure 43 FAN Signal Cable

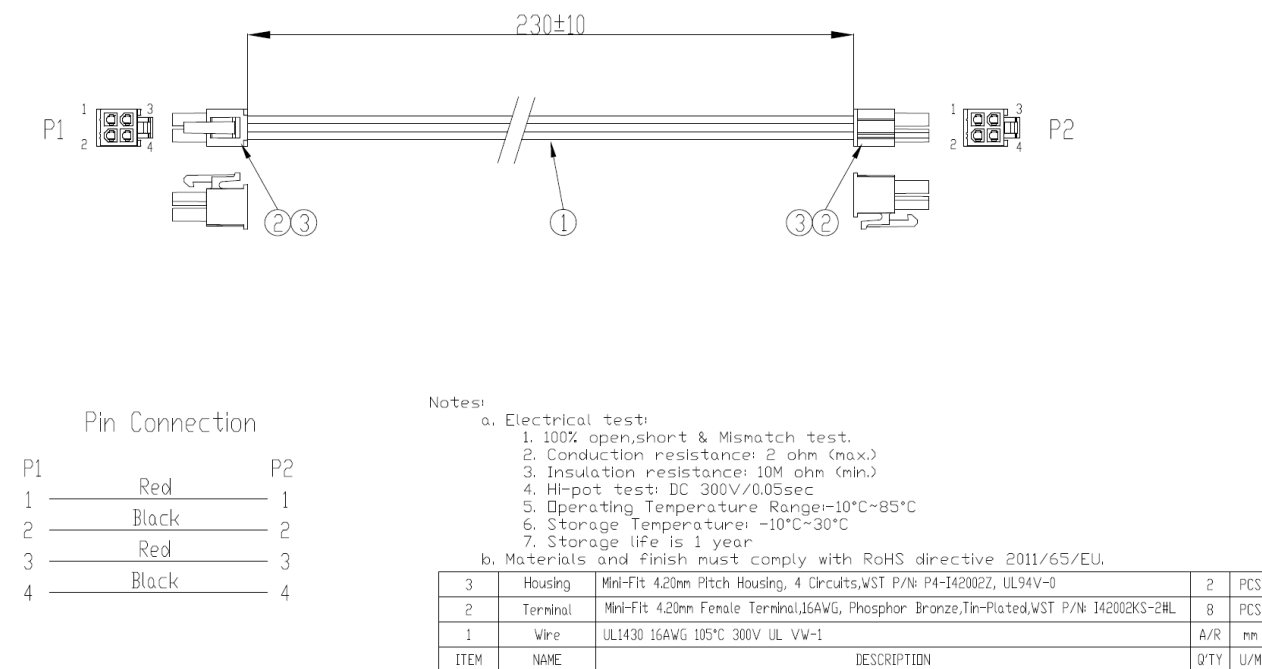


Figure 44 FAN Power Cable

5.3. Placement

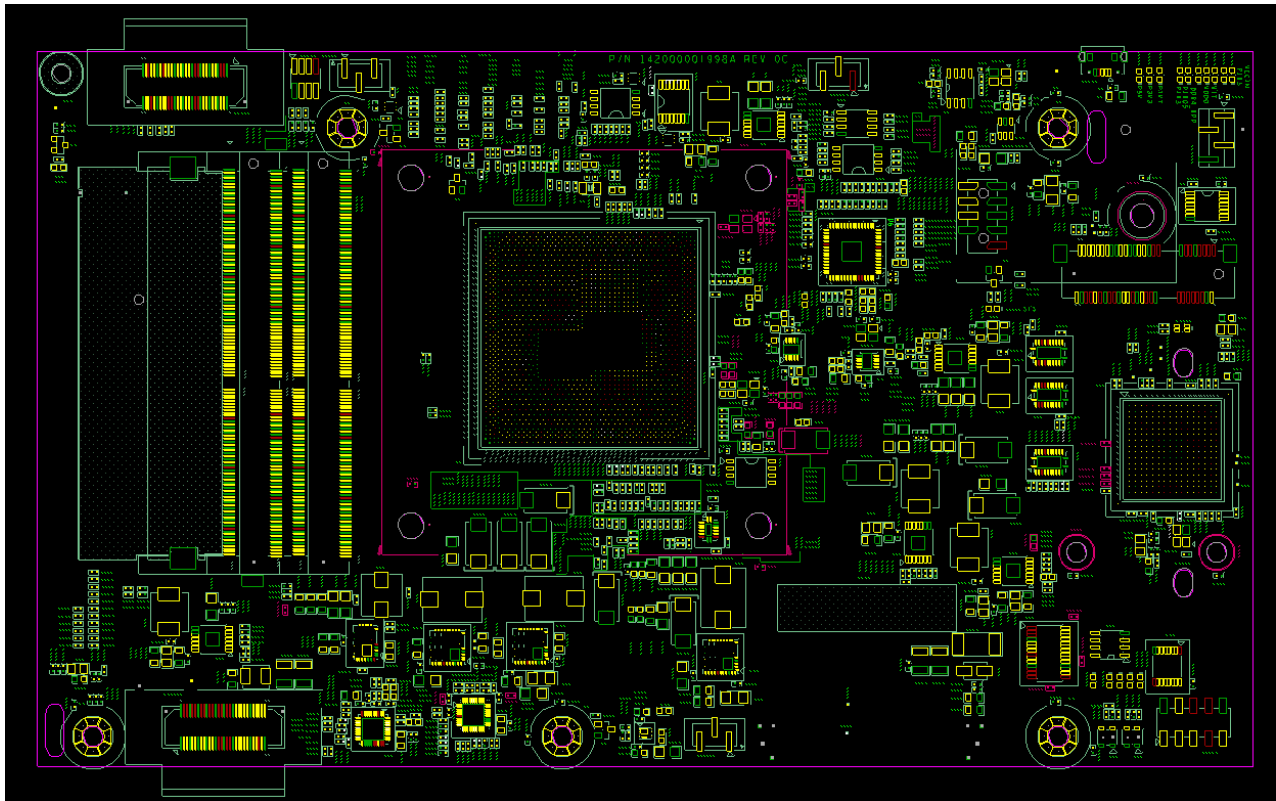


Figure 45 CPU PCB Placement

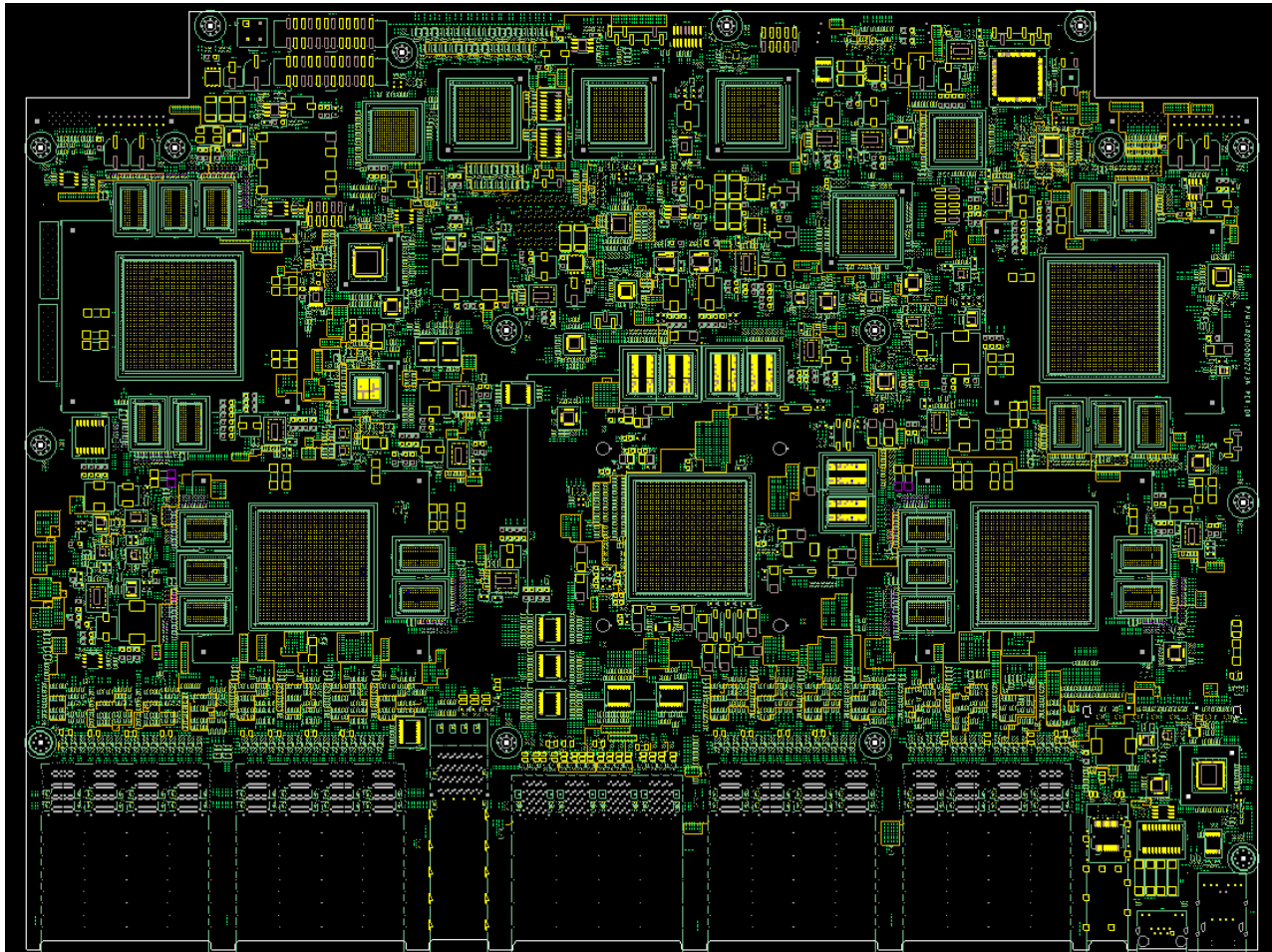


Figure 46 Mainboard TOP PCB Placement

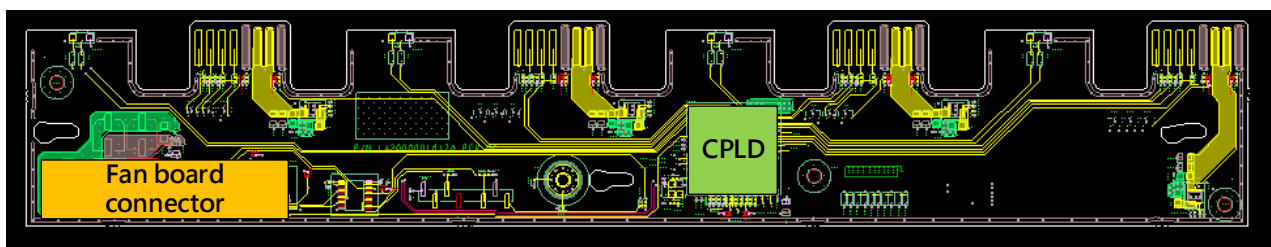


Figure 47 FAN board TOP/Bottom PCB Placement

6. Mechanical

Height: 89mm (Maximum)

Width: 477mm

Depth: 600mm

6.1. Dimension

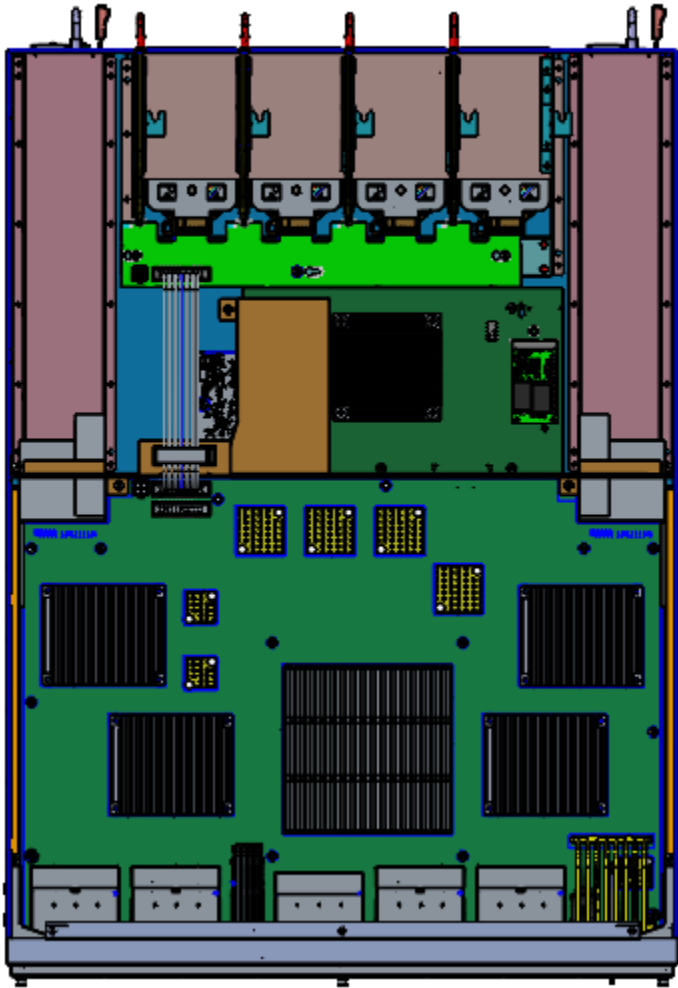


Figure 48 Mechanical Dimension



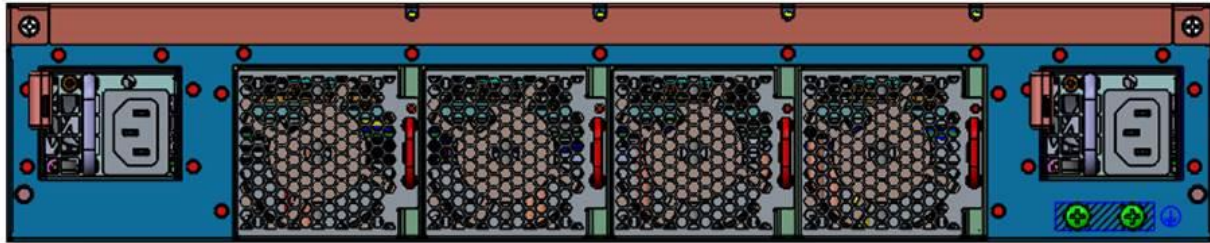


Figure 49 Mechanical Front/Back view

6.2. Placement

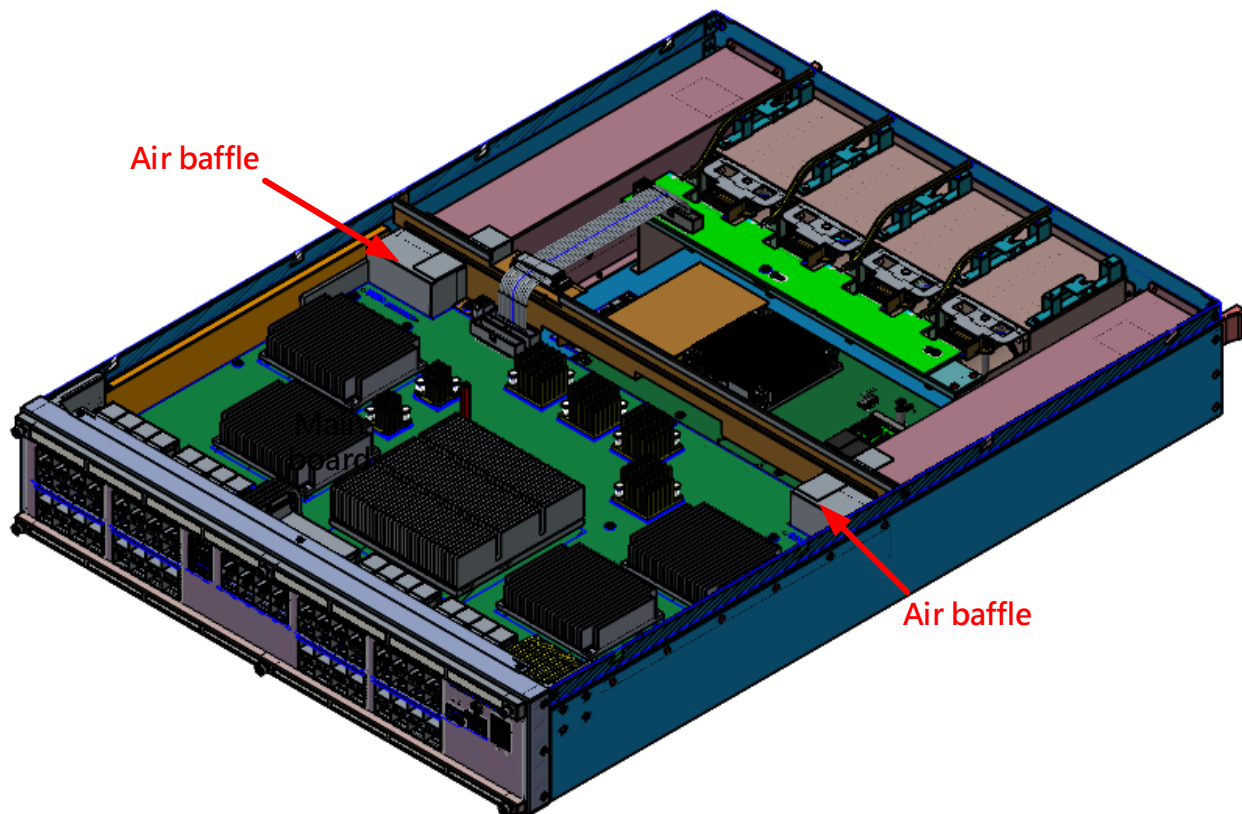


Figure 50 Mechanical Placement

6.3. Cooling Method

6.3.1. Fan module

System supports below Fan module.

- Front to back Fan module with red color handle
- Back to Front Fan module with blue color handle

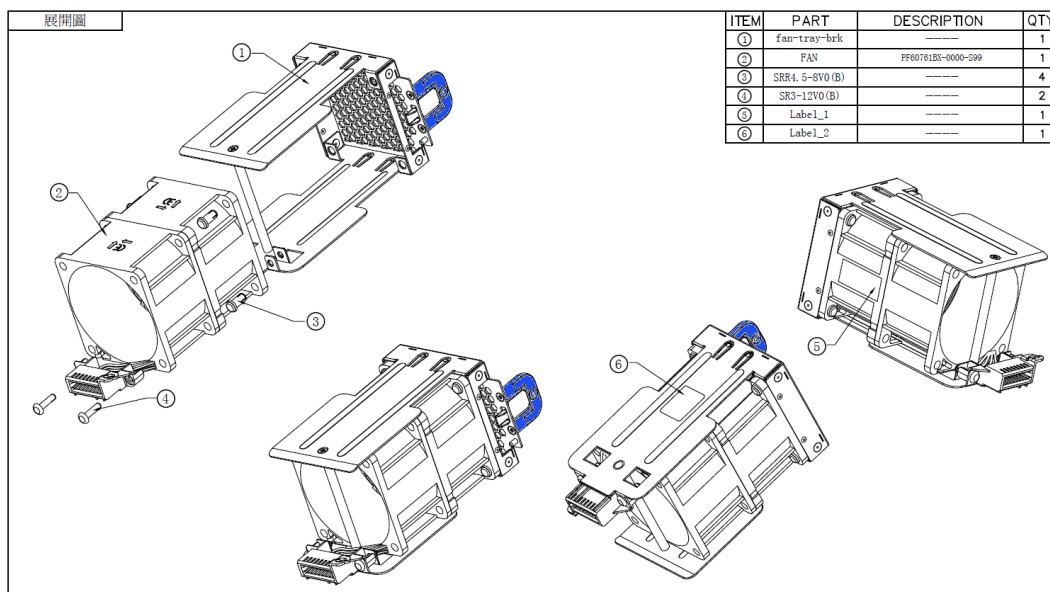


Figure 51 Back to front fan module

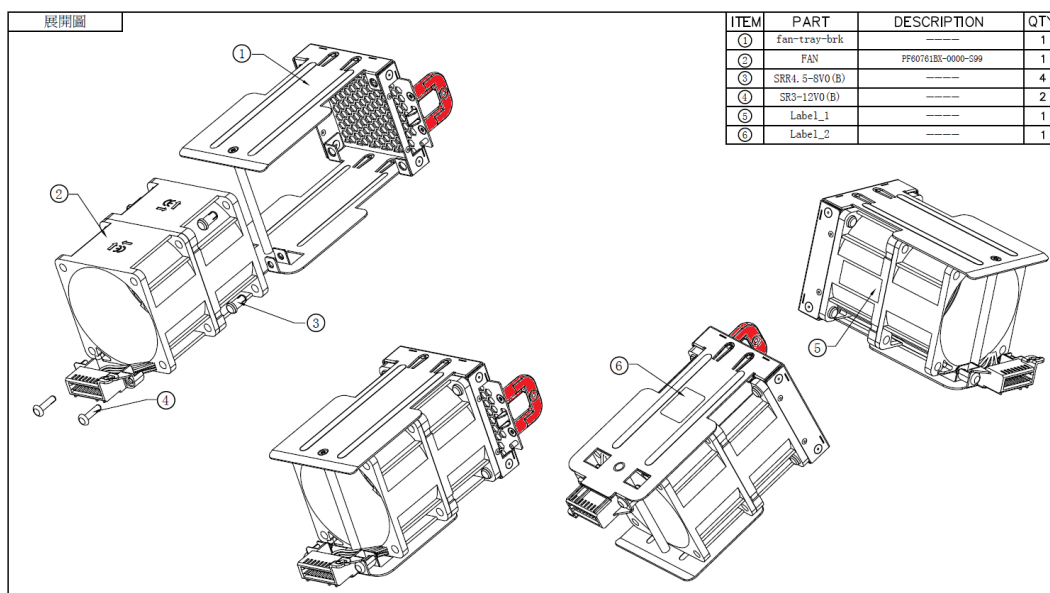


Figure 52 Front to Back fan module

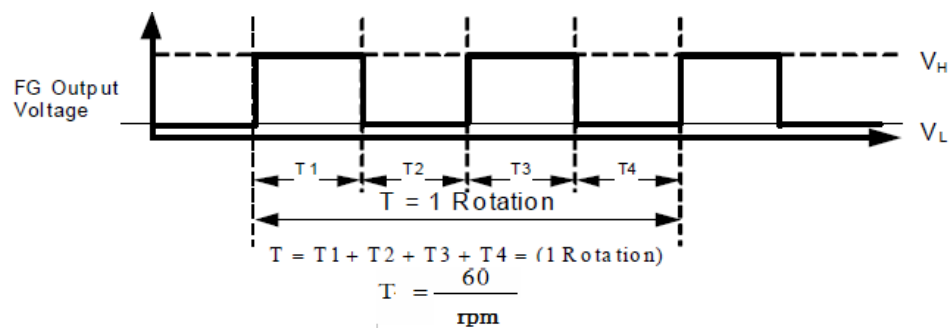
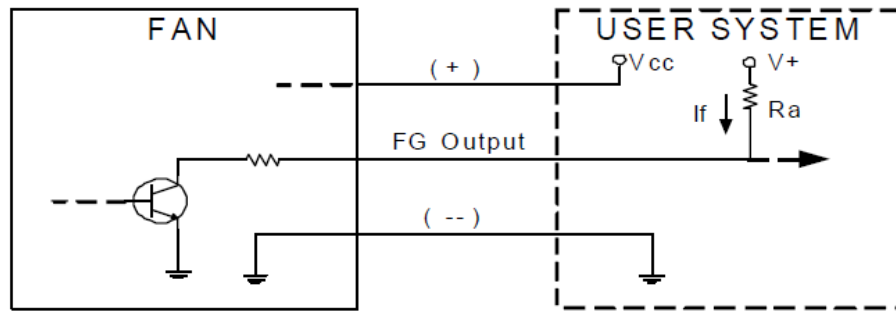
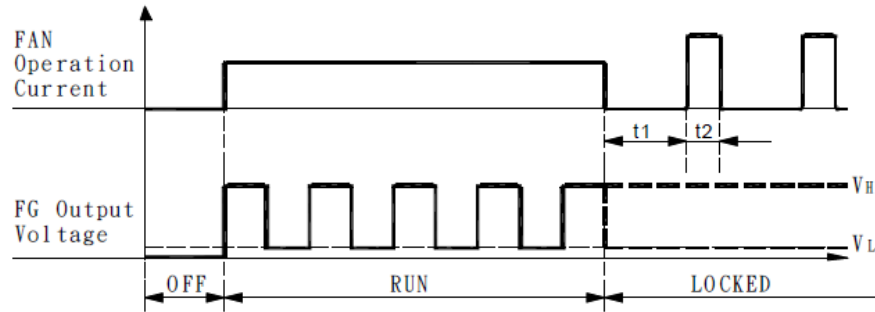


Figure 53 Fan Speed information



$$*Ra \geq V^+ / If (\max)$$



★Electrical Characteristics : (at Ta = 25°C) Vcc=12V

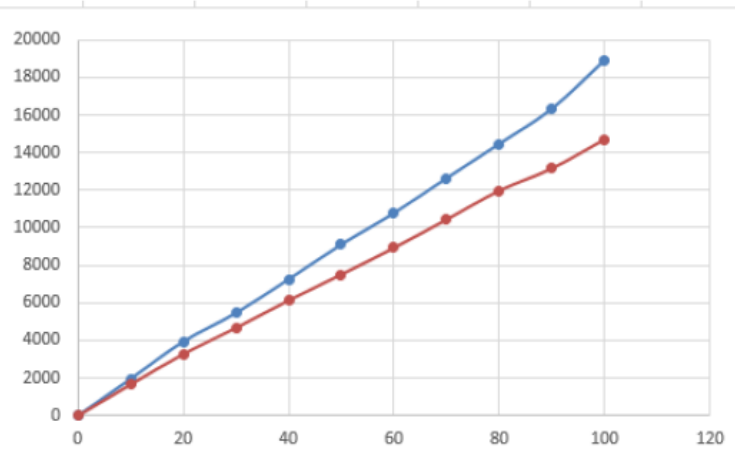
Parameter	Ratings			Unit
	min	typ.	max	
FG Supply Voltage(V+)	3	--	13.2	Voltage
FG Output Current (If)	--	--	5	mA
FG Output (VL)	--	--	0.5	Voltage
FG Output (VH)	--	V+	--	Voltage
Ratio(=t1/t2)	--	11	--	

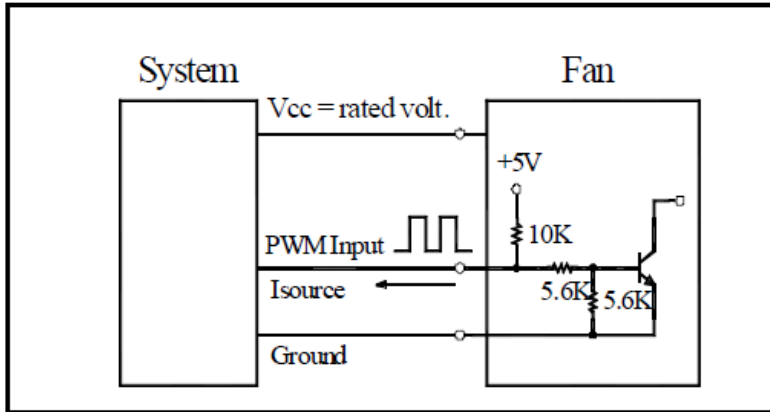
Figure 54 Fan failed information

FAN Module: INVNI PF60761BX-0000-S99

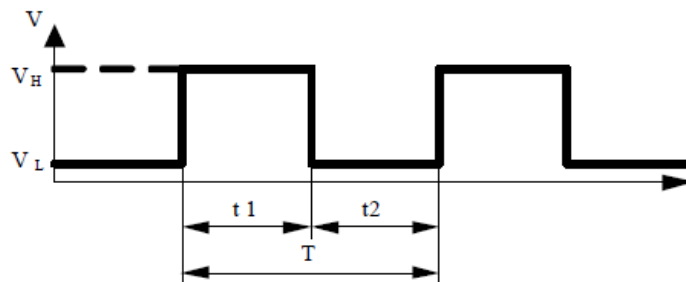
FAN SPEC (Duty Cycle ⇔ PWM)

FAN	SPEED (RPM)	
Duty Cycle	IN	OUT
0	0	0
10	1959	1660
20	3945	3275
30	5464	4670
40	7257	6129
50	9108	7510
60	10780	8925
70	12636	10437
80	14464	11965
90	16332	13150
100	18919	14702





★PWM INPUT WAVEFORM



1. Period :
$$T = \frac{1}{f_{PWM}} = t_1 + t_2 (\text{sec})$$

2. Duty Cycle (D.C.) :
$$\frac{t_1}{t_1 + t_2} * 100 = \frac{t_1}{T} * 100 (\%)$$

3.PWM Duty Cycle VS Speed (at Ta = 25°C, Vcc =12VDC, fpwm=25KHz)

PWMDuty Cycle (%)	Inlet (R.P.M.)	Outlet (R.P.M.)
100	18200rpm ±10%	14700rpm ±10%
50	9100rpm ±10%	7350rpm ±10%

★ Electrical Characteristics at Ta = 25°C ; Vcc=12V

Parameter	Min	Typical	Max	Unit
f pwm	5k	25k	40k	Hz
V _H	2.3	—	5.5	V
V _L	0	—	0.8	V
Isource	—	1	—	mA
D.C.	0	—	100	%

* The speed is default to be maximum if PWM input pin is unconnected.

* Min start up duty cycle is 10%. Please don't apply 1 ~ 9% duty cycle to prevent unstable fan speed.

Figure 55 Fan PWM

The Nuage system only can provide 3.3V PWM signal. The min of V_H of fan need be low than 3.3V.

6.3.2. Heat-Sink Design

For MAC the heat-sink dimension will be 110x110x30mm and mounting by screw.

The detail is shown as below.

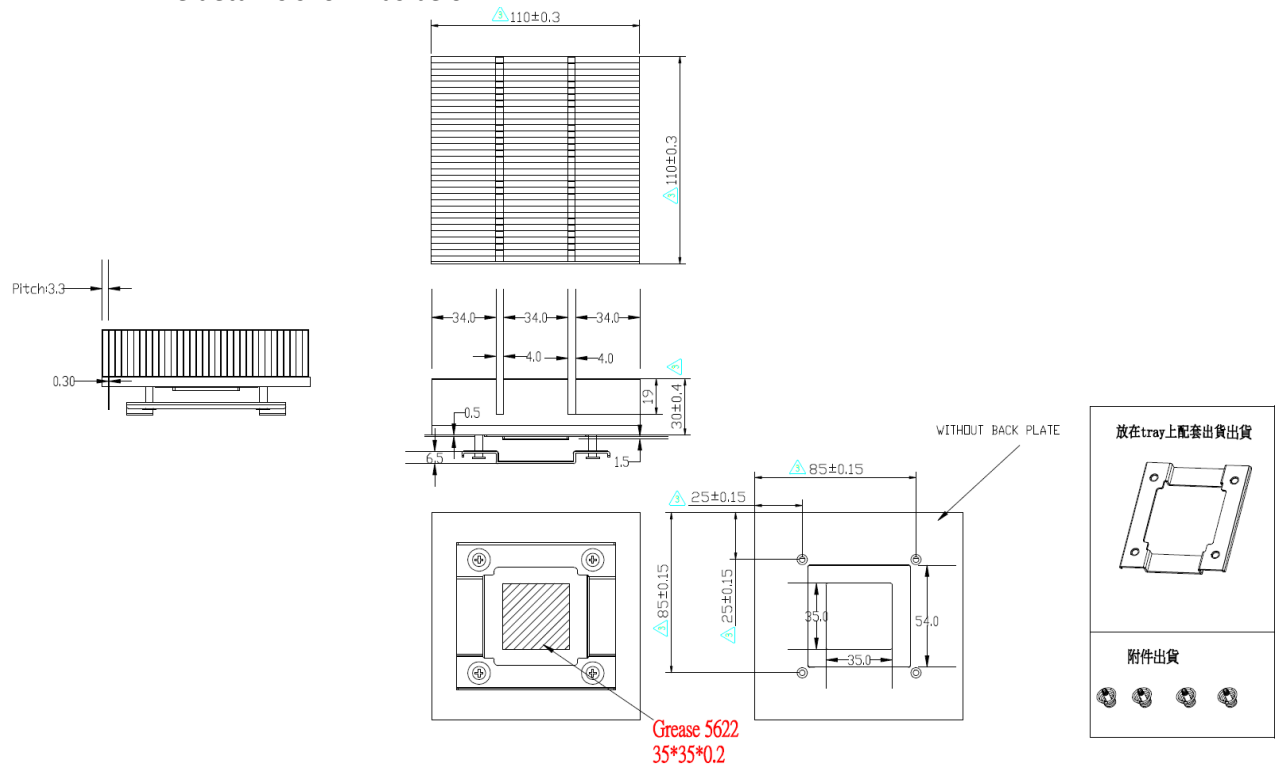
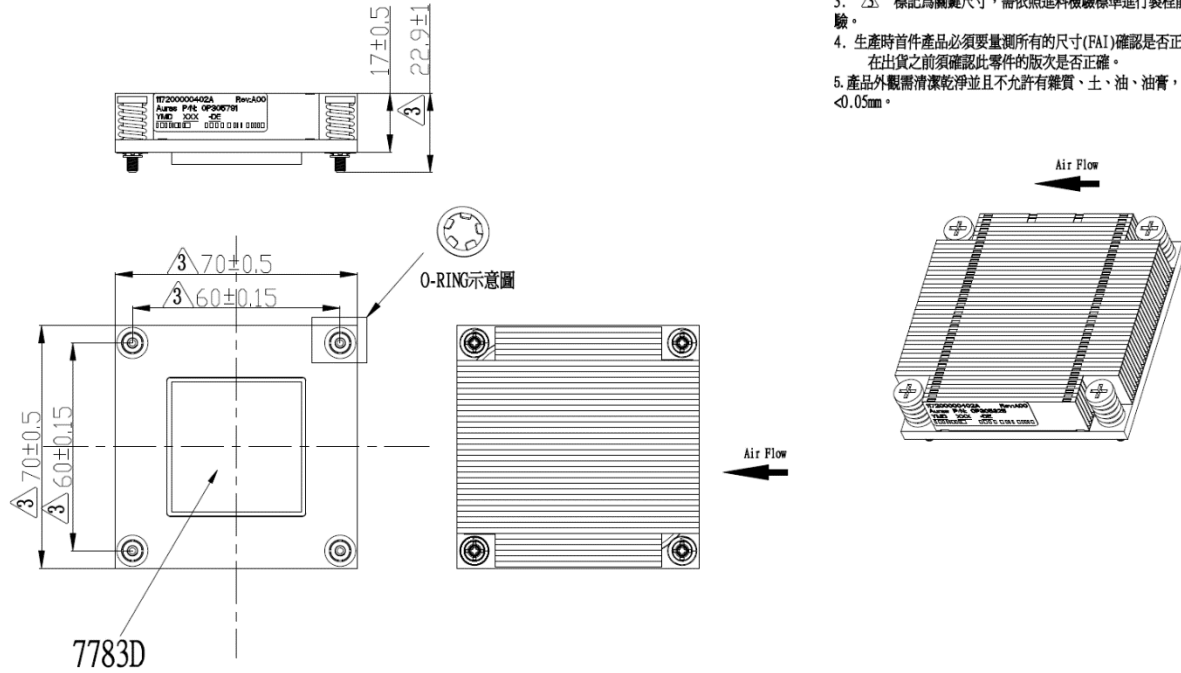


Figure 56 MAC Heat-sink View

For CPU heat-sink dimension will be 70x70x17mm and mounting by push type.
The detail is shown as below.



註釋:

1. 所有尺寸公差是依據美國國家標準學會所制定。
2. 所有零件都必須符合RoHS2.0及無鹵素規範。
3. "△" 標記為關鍵尺寸，需依照進料檢驗標準進行製程能力(CP, CPK)檢驗。
4. 生產時首件產品必須要量測所有的尺寸(FAI)確認是否正確。
在出貨之前須確認此零件的版次是否正確。
5. 產品外觀需清潔乾淨並且不允許有雜質、土、油、油膏，且披鋒毛刺 < 0.05 mm。

Figure 57 CPU Heat-sink View

7. MISC

7.1. Push Button

Push Button is on mainboard which is H/W Reset function used.

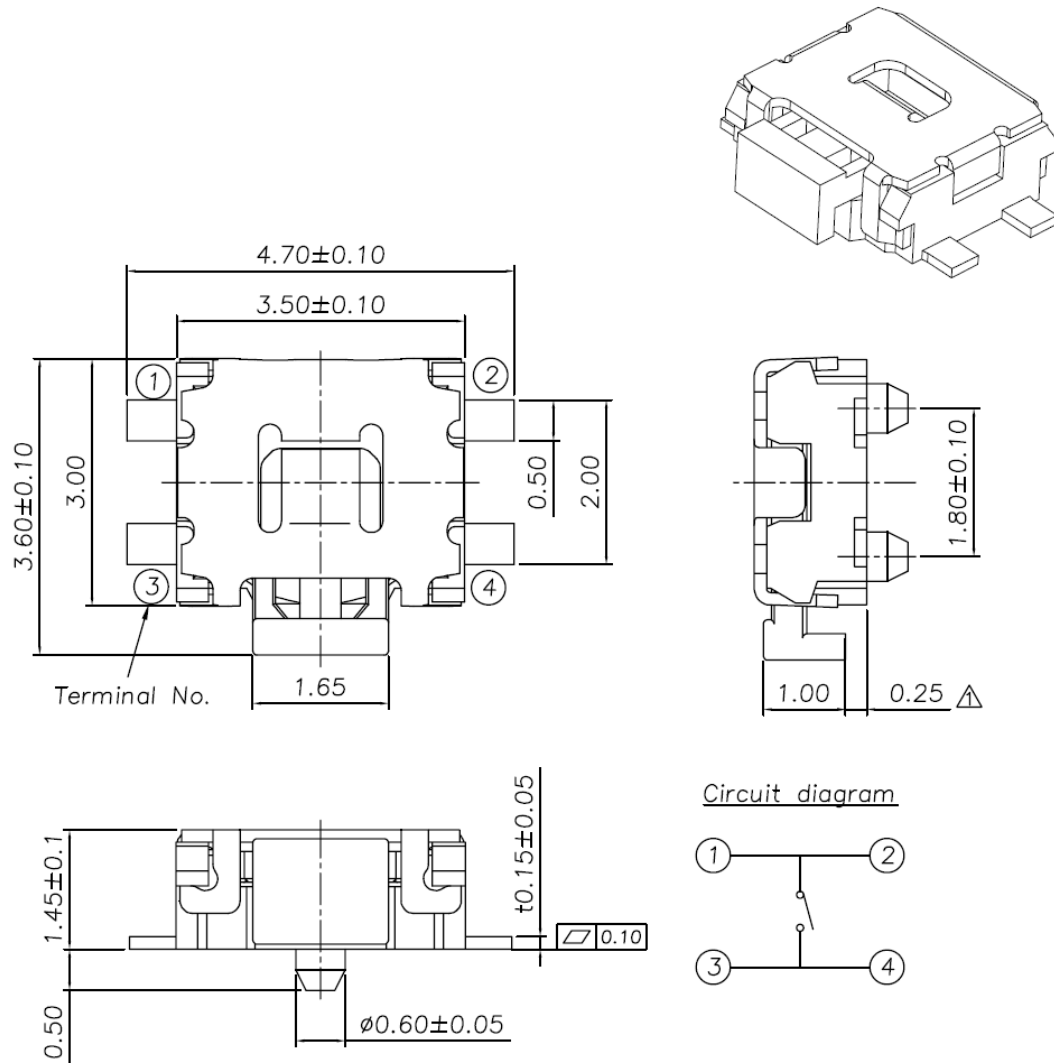
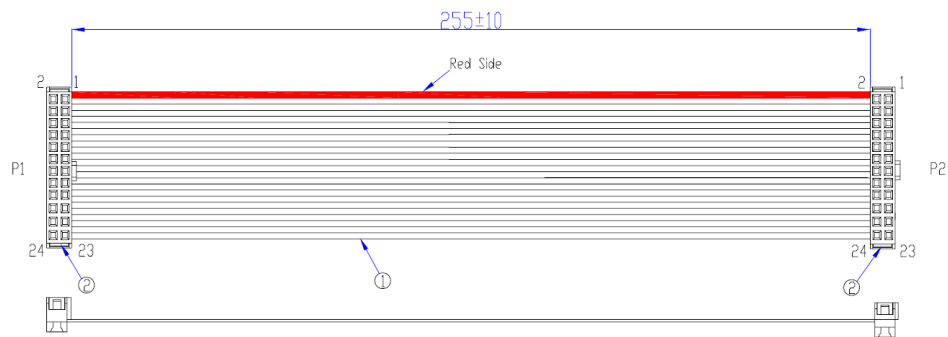


Figure 58 Push Button Dimension



Figure 59 Push Button Location

7.2. Cable



Pin Connection

P1		P2
1	Red	1
2	Grey	2
3	Grey	3
	⋮	
22	Grey	22
23	Grey	23
24	Grey	24

Notes:

- Electrical test:
 - 100% Open & Short & Mismatch test.
 - Conduction resistance: 2 ohm (max.)
 - Insulation resistance: 10M ohm (min.)
 - Hi-pot test: DC 300V/10ms
 - Operating Temperature Range: -10°~80°C
 - Storage temperature: -10°C~20°C
- Materials and finish must comply with RoHS directive 2011/65/EU.

2	Housing	254mm IDC Connector With Nose, 2x12 Poles, Black, 三井式	2	PCS
1	Cable	UL2651 28AWG 24Pins, Pitch 1.27mm, Grey with Red Marking on 1st conductor Ribbon Flat Cable	1	PCS
ITEM	NAME	DESCRIPTION	Q'TY	U/M

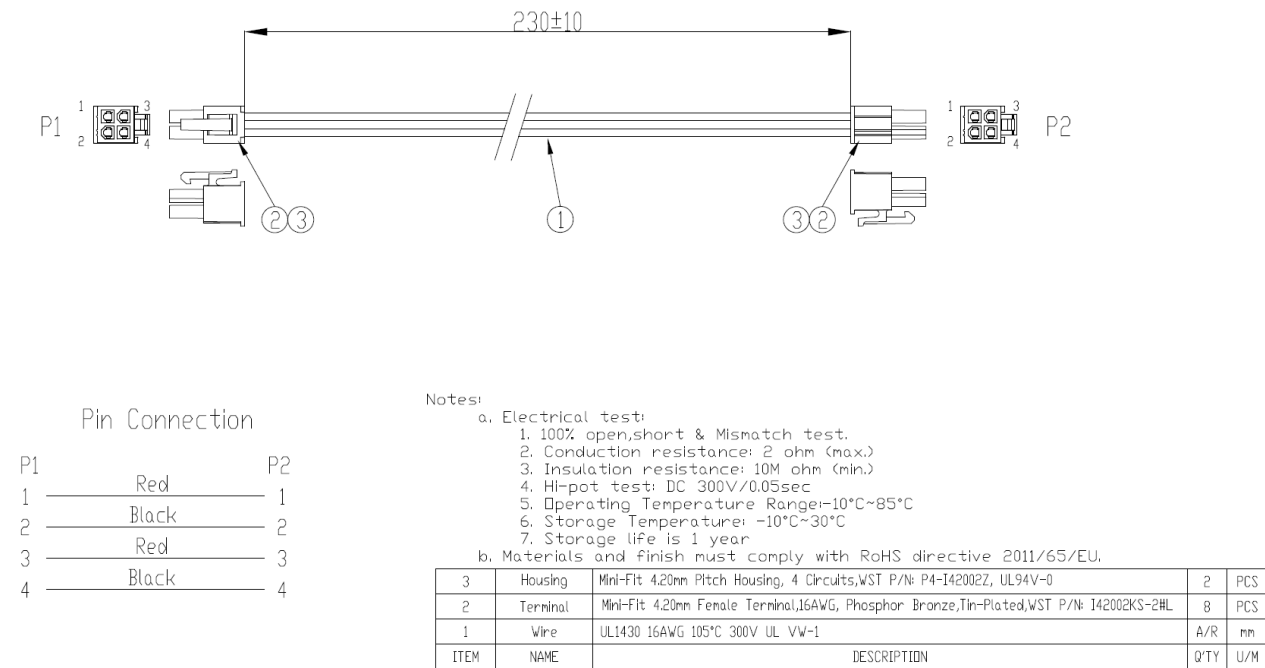


Figure 60 Mainboard to FAN board Cable

8. Specifications and Standards

8.1. Safety

- CE certification
- UL/ Canada
- CB (Issued by TUV/RH)
- China CCC
- Grounding & electrical safety of: ETSI EN 300 253, DIN VDE 0800, Part 2, DIN EN50310 and DIN EN50174-2.
- Labeling (input voltage range, frequency, max. input current) according to DIN EN60950-1; FRU labeling requires to state for BASE product, FAN Assemblies and Power Supplies.
- Cables and the individual conductors (e.g., for power supply, equipotential bonding) must be marked in accordance with DIN EN 60445 (VDE 0197) and DIN EN 60446 (VDE 0198).

8.2. Electromagnetic Compatibility

- CE Mark
 - ▶ EN55022 Class A
 - ▶ EN55024 (Immunity) for Information Technology Equipment
 - ▶ EN61000-3-2
 - ▶ EN61000-3-3
- North America: FCC Title 47, Part 15, Subpart B Class A
- Japan: VCCI Class A
 - GR-1089-CORE
 - European standards for Electro Magnetic Compatibility : EN 300 386 in conjunction with EN 55022 (Class A) / EN 55032 (Class A)
- ITU-T K.20, K.21

8.3. Environmental

Environmental placement requirements differ for the outdoors and indoors units.

It is not expected that a high port-count OLT is deployed in an outdoor scenario. The specification shall nevertheless not preclude the implementation of an outdoor version of this OLT.

Temperature and Humidity Operating Requirements:

Conditions	Limits
Operating Temperature*	+5°C to 40°C*
Operating Temperature Short-term*	-5°C to 55°C (F2B case only)
Operating Temperature Fan-fail	-5°C to 40°C
Storage temperate range	-40 to 40°C
Rate of Temperature Change	30°C / hr
Operating Relative Humidity	5% to 85%
Operating Relative Humidity Short-term*	5% to 93°C

Dew Point	17°C
-----------	------

- Vibration – IEC 68 - 2 - 36, IEC 68 - 2 - 6
- Shock – IEC 68 - 2 - 29
- Acoustic Noise Level –
 - Comply based on ETS 300 753, the environmental class is for 3.1. That is 72dB(A) per device @23 ± 2°C
 - Comply with NEBS GR63-CORE ISSUE 4, section 4.6. That is 78dB at 27°C
- Altitude - 15,000 (4572 meters) tested operational altitude

8.4. ROHS (6/6) Requirement

Restriction of Hazardous Substances (6/6):

Compliance with Environmental procedure 020499-00, primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC).

Software Support

The ASGvOLT-64 supports a base software package composed of the following components:

BIOS support

The ASGvOLT-64 Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

ONIE

See <https://github.com/opencomputeproject/onie/tree/master/machine/accton> for the latest supported version

Open Network Linux

See <http://opennetlinux.org/> for latest supported version